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Publication Number 0117-0274-10

August 1984

K105-D LOGIC ANALYZER

SERVICE MANUAL

Gould, Inc., Design & Test Systems Division
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8/84

WARNING

This equipment has not been tested to show compliance with new FCC Rules (47 CFR Part 15) designed to limit interference to radio and TV reception. Operation of this equipment in a residential area is likely to cause unacceptable interference to radio communication requiring the operator to take whatever steps are necessary to correct the interference.

The following procedures may help to alleviate the radio or television interference problems:

1. Reorient the antenna of the receiver receiving the interference.

2. Relocate the equipment causing the interference with respect to the receiver (move or change relative position).

3. Reconnect the equipment causing the interference into a different outlet so the receiver and the equipment are connected to different branch circuits.

4. Remove the equipment from the power source.

NOTE:

The user may find the following booklet prepared by the FCC helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402. Stock Number 004-000-00345-4.

PREFACE

This manual contains information for servicing and maintaining the Gould K105-D Logic Analyzer. Procedures are provided for making adjustments and calibrating the control circuits for various functions. These procedures include the use of diagnostic tests to troubleshoot and isolate a malfunction to a circuit component. Theory of operation is presented for the printed circuit board functions. Service aids in the form of schematic diagrams, assembly drawings, cable connection diagrams and parts lists are included for user reference.

The material in this manual reflects the Control Firmware level valid on August 1, 1984, and is up-to-date at the time of publication, but is subject to change without notice.

Copies of this publication and other Gould, Inc., Design and Test Systems Division Publications may be obtained from the Gould, Inc., Design and Test Systems Division sales office or distributor serving your locality.

RELATED PUBLICATIONS

The following support documentation may be used in conjunction with this manual:

> K105-D User's Manual, Publication Number 0117-0014-10 which describes the capabilities, functions and operation of the K105-D Logic Analyzer.

ASSISTANCE

If you require assistance on this product, please call Gould, Inc., Design and Test Systems Division Customer Service on the toll-free, hot-line number listed below:

Nationwide (800) 538-9320/21

California (800) 662-9231

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0117-0055	Threshold/Clock Board Assembly
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0117-0060	Trace Control Board Assembly
0117-0061	Trace Control Board Schematic
0117-0070	High Speed Timing Board Assembly
0117-0071	High Speed Timing Board Schematic
0117-0075	I/O Board Assembly
0117-0076	I/O Board Schematic
0117-0145	Data/M-Memory Board Assembly
0117-0146	Data/M-Memory Board Schematic
0114-0185	MPU Board Assembly
0114-0186	MPU Board Schematic
0114-2010	Data Display Board Assembly
0114-2011	Data Display Board Schematic
0117-0377	Power Supply Schematic
0117-0021	CRT Cable Assembly
0117-0099	Probe Subassembly
0117-0117	Power Switch Cable Assembly
0117-0124	Fan Harness Assembly
0117-0128	Main Channels Cable Kit
0117-0133	Chassis Ground Cable
0117-0144	Mother Board Harness
0117-0157	RS-232C Harness Assembly
0117-0158	IEEE-488 Harness Assembly
0117-0165	+/-5 Volt Harness Assembly
0117-0167	DOS Option Assembly
0117-0170	DOS Power Harness Assembly
0117-0221	5.2 Volt Mother Board Cable Assembly
0117-0222	15 Volt Mother Board Cable Assembly
0117-0223	High Speed Cable Kit

GENERAL DESCRIPTION

INTRODUCTION

The Gould Model K105-D Logic Analyzer is a precision test instrument that monitors input logic signals generated by the user's external microprocessor based equipment. The K105-D accepts inputs from either 32 or 64 main data inputs which can be accompanied by 16 or 8 high- speed data inputs, respectively. Figure 1-1 illustrates and describes the seven main and high-speed input combinations possible with the K105-D.

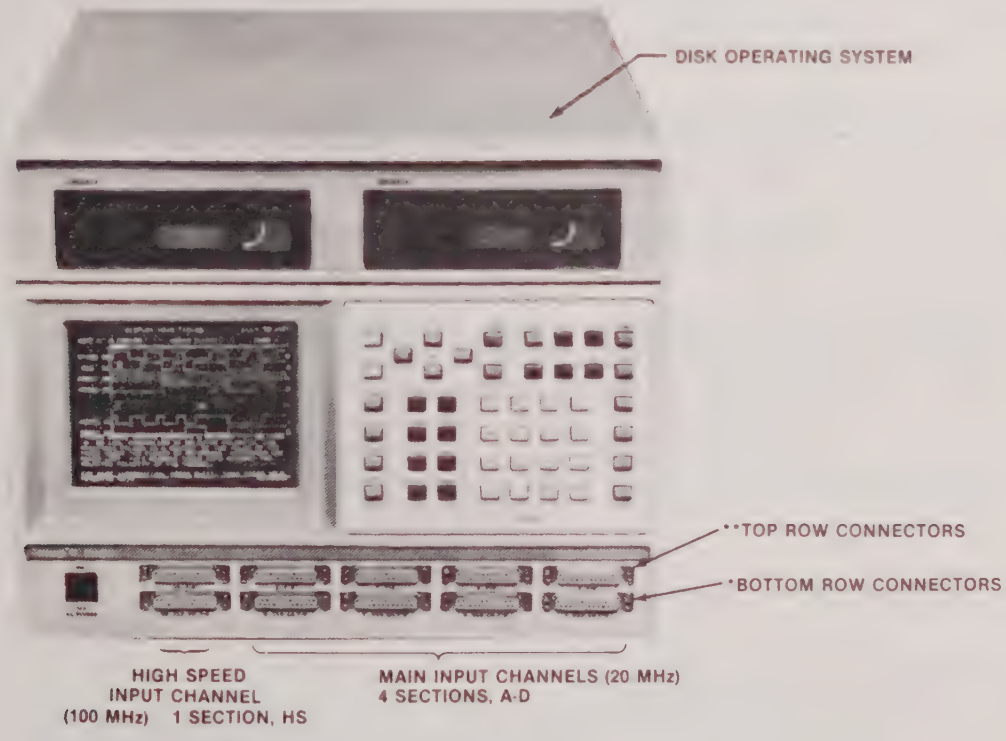


Figure 1-1. K105-D Logic Analyzer Input Configurations

The K105-D internal control logic examines the data input signals to accomplish comparison analysis, capture data samples, correlate data characteristics and record the results in memory. The K105-D uses menu-driven firmware which is controllable via function keys on the front panel. The menu displays allow the user to easily set up criteria for the examination of data and the capture and display of data.

Overview of Manual Contents

The organization and scope of this manual describes the K105-D circuit characteristics and component functions as applicable for servicing and calibrating the unit to maintain its accuracy and availability for use. Service aids in the form of schematic diagrams, assembly drawings, cable connection drawings and diagrams, and parts lists are included for reference purposes. The manual content is arranged as follows:

Chapter 1. GENERAL INFORMATION - This chapter presents an overview of the K105-D operating features, organization of manual contents, servicing philosophy, maintenance features and equipment specifications.

Chapter 2. SYSTEM COMPONENTS AND INTERCONNECTION - This chapter describes the interconnection of printed circuit boards, power distribution, external I/O interface, and necessary tools and test equipment.

Chapter 3. CALIBRATION AND POWER UP DIAGNOSTICS - This chapter describes the calibration of the Data Display and Threshold/Clock boards and the power up Boot PROM diagnostics.

Chapter 4. THEORY OF OPERATION - This chapter presents theory of operation for circuitry contained on each board of the K105-D.

Chapter 5. DOS DIAGNOSTICS - This chapter presents a description of each diagnostic module and its associated subtests. Instructions are included for interpreting the results of the subtests.

Chapter 6. SCHEMATIC DIAGRAMS AND PARTS LISTS - This chapter provides reference material such as schematic diagrams, assembly drawings and parts lists.

SERVICING PHILOSOPHY

Maintenance strategy for the K105-D involves the use of diagnostic routines to isolate a defecttve circuit board. These diagnostic routines are contained in PROM and on diskette. In the case of the diagnostics residing in the PROM, these diagnostics are performed upon power-up of the K105-D and provide an indication of the disk diagnostic that should be performed in the event of a failure. Descriptions of the power-up diagnostics are contained in Chapter 3 of this document. The diagnostics contained on disk perform a wide range of tests as described in Chapter 5 of this manual.

The use of any diagnostic aids for troubleshooting does not preclude the need for user interaction to visually inspect cable connections, ensure proper seating of printed circuit boards and that calibration adjustments fall within prescribed limits. After completion of a repair, diagnostics should again be performed prior to placing the unit in operation.

SPECIFICATIONS

The following is a summary of the physical, environmental and operating characteristics of the K105-D.

Power Requirements

Input Frequency: 50-60 Hz
Input Voltage: 90-135 VAC or 180-270 VAC
Input Power: 250 Watts without DOS option, 300 Watts with DOS option

Fuses for rated voltage:	Voltage Range	Fuse
	90 VAC to 135 VAC	3AG, 6 Amp
	180 VAC to 270 VAC	3AG, 3 Amp

Physical Dimensions and Weight

Height: 8.5 inches (21.8 Cm) without DOS, 12 inches (30.1 Cm) with DOS
Width: 17.5 inches (44.5 Cm)
Depth: 24.7 inches (62.7 Cm) including handle

Weight: minimum system - 35 lb. (15.9 Kg)

1.0 lb. (.45 Kg) per additional board
15.0 lb. (7.0 Kg) for DOS option
8.5 oz. (240 grams) per probe

Environmental Limits

	Operating	Storage
Ambient Temperatures:	32° to 122°F(0° to 50°C)	-8° to 117°F(-20° to 50°C)
Relative Humidity:	20% to 80%	1% to 95%
Max. Wet Bulb:		

Loading Characteristics

Signal Inputs:

Input Resistance: 1 megohm referenced to threshold
Input Capacitance: <= 6 pF

NOTE: Input resistance may approach 500K ohms at voltages exceeding +/-15 volts from threshold.

Maximum input without damage: +/-50 volts peak

Common mode rejection: +/-0.5 volt max between probe and unit probed

Transfer Characteristics

Bandwidth: >100MHz

Min. swing for output: threshold -0.20 V maximum

Threshold variance: +/-15 MV max, input to input
+/-30 MV max, any two probes

Main Inputs

32 (or 64) main inputs contained in four sections (A, B, C, D) of 8 (or 16) sample inputs each.

Input modes: two modes, Sample and Demultiplex

Sample input frequency: 20MHz

High Speed Inputs

8 (or 16) high speed inputs contained in a single section, HS

Input modes: two modes, Sample and Glitch

Sample input frequency: 100MHz

Main Clocks

Internal: Clock is selectable from 50ns (20MHz) to 50 ms (20Hz) in a 1, 2, 5 sequence

One internal clock may be programmed per recording

External: Eight external clock inputs which may be combined to form four sample clocks and one master clock

Maximum clock frequency for this mode is 20MHz

Minimum detectable pulse width: 25ns

Skew between clocks: 15ns, typical

High Speed Clocks

Internal: Clock is selectable from 10ns (100MHz) to 50ms (20Hz) in a 1, 2, 5 sequence

External: Two external clocks, HJ and HK, are available as inputs and are ORed together. Each clock input is selectable as a rising or falling edge, or is not used

Minimum detectable pulse width: 7ns

Skew between clocks: 2ns, typical

Signal Outputs

VIDEO OUT BNC connector output: 1v p-p into 75 ohms RS-170 compatible levels

MASTER CLOCK BNC connector output: TTL compatible

LINK (Trigger) BNC connector output: TTL compatible

+/-5VDC LEMO connector outputs: Two each accessory power connectors rated at +5V and -5.2V @ 300MA

Setup and Hold

Data must be present 25ns before clock active edge

Data must be present 0ns after clock active edge

Minimum detectable pulse width is one clock period +25ns

Trace Memory

For each data board, trace memories M, A and B are 36 bits wide by 1024 bits deep; 32 bits store data, and four bits store trace levels.

Interface

Floppy disk storage system for setups and measurements

1 IEEE-488/1978 port for Talker/Listener interface

1 RS-232 I/O port for control and printer output

1 Auxiliary I/O port (RS-232, but not presently supported)

SYSTEM COMPONENTS AND INTERCONNECTIONS

INTRODUCTION

This chapter describes the individual boards and components that comprise the K105-D. Further descriptions are included for the interconnection of these boards and components, and the equipment necessary for repair of the K105-D. Figure 2-1 illustrates the locations of the boards in the card cage.

BOARDS AND COMPONENTS

The boards and components that make up the K105-D are listed as follows:

- Keyboard--The keyboard, configured as a scanned matrix, consists of 48 keys, many of which can be shifted to perform a second function. Because of the shift function, 20 keys can perform as a full alpha-numeric keyboard. Also present on the keyboard is the power LED. When illuminated, this LED indicates the presence of +5 VDC.

- Front Connector Panel--The front connector panel comprises ten DB-25 female connectors and the AC power switch. The connectors that are active for any specific unit depend on the boards present in that machine. The machine can be configured with any combination of three input boards consisting of up to two Data boards and up to two High Speed Timing boards. The configuration display defines the active connectors.

- Display Assembly--The display assembly consists of a C822P39 CRT and a CRT deflection yoke with cable harness. The mounting bracket for the assembly is an integral part of the CRT glass envelope.

- Rear Connector Panel--The rear connector panel provides outputs for video, master clock and the link signal via BNC connectors. Two sets of +/-5 VDC outputs are also provided via the LEMO connectors. Interface connectors consist of one IEEE-488 connector and two RS-232 connectors (only one of which is currently supported).

- Power Supply--The power supply is a switching type supply providing the following outputs:

  +5 VDC at 30 Amps
  -5.2 VDC at 5 Amps
  +12 VDC at 2 Amps
  +15 VDC at 1.3 Amps
  -15 VDC at 1 Amp

- Data Board--The Data board interfaces the ECL devices of the probes to the TTL devices of the board and processes 32 main inputs.

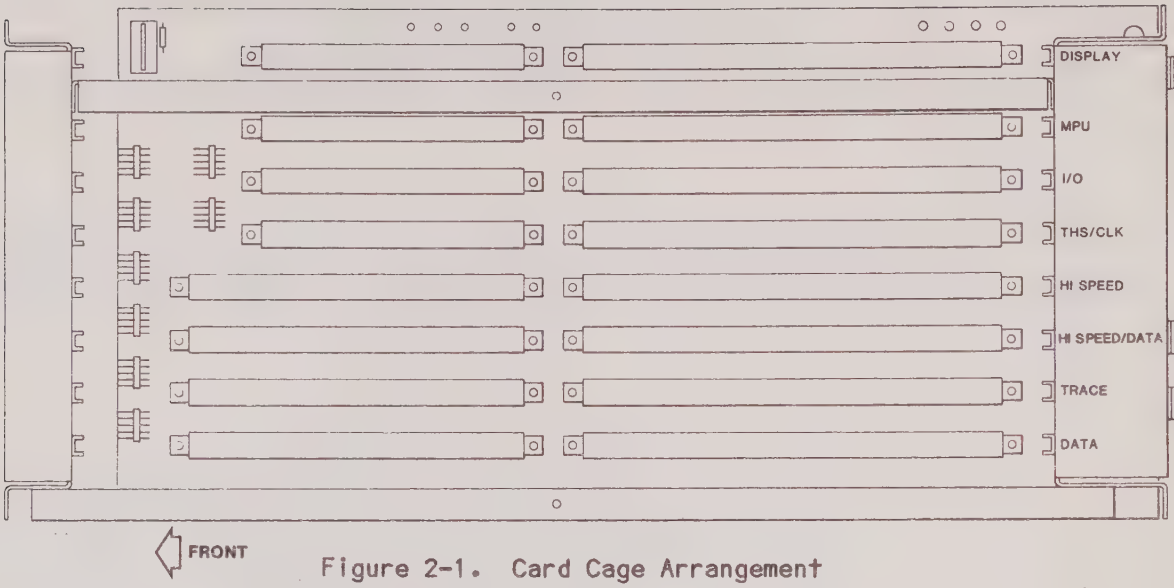


Figure 2-1. Card Cage Arrangement

The Data board memory is 1K bits deep by 32 bits wide and gathers data at 20MHz.

- MPU Board--The MPU board contains an 8086 microprocessor and operates as the controller for the K105-D. The operating firmware resides in ROM on the MPU board.

- Trace Control* Board--The Trace Control board provides the user with eight trace levels to be programmed. A selection of qualifiers enables the user to pick and choose the information he wishes to record.

- Threshold/Clock Board--The Threshold/Clock board provides fixed and variable threshold voltages for the probe pods. In addition, this board also processes the external clocks from the pods and provides a range of internal clocks for the system.

- I/O Board--The I/O board provides interface for the following:

  Two RS-232 ports (only one is currently supported)
  One IEEE-488 Talker/Listener port
  Two 5 1/4" floppy disk drives

- Data Display Board--The Data Display board contains the keyboard scanning circuitry and the horizontal and vertical deflection and high-voltage circuitry for the CRT.

- High Speed Board--The High Speed board has one level of triggering and processes inputs at 100MHz. The memory for this board is organized as 1K by 8-bits.

BOARD AND COMPONENT INTERCONNECTIONS

Boards

The K105-D printed circuit boards are contained in an eight-slot card cage, and are interconnected via a mother board. Interconnection of the printed circuit boards with the front and rear connector panels is accomplished through flat-cables that mate to connectors located along the upper edges of the printed circuit boards. Figure 2-2 is a block diagram illustrating the interrelationships of the boards.

Components

Because the K105-D is a compact unit, the discrete cable harnesses necessary to connect the power supply to the mother board and the display assembly to the Data Display board are kept quite short. The mother board is connected to the keyboard by a short flat-cable.

*Trace Control is a registered trademark of Gould Electronics, Inc.

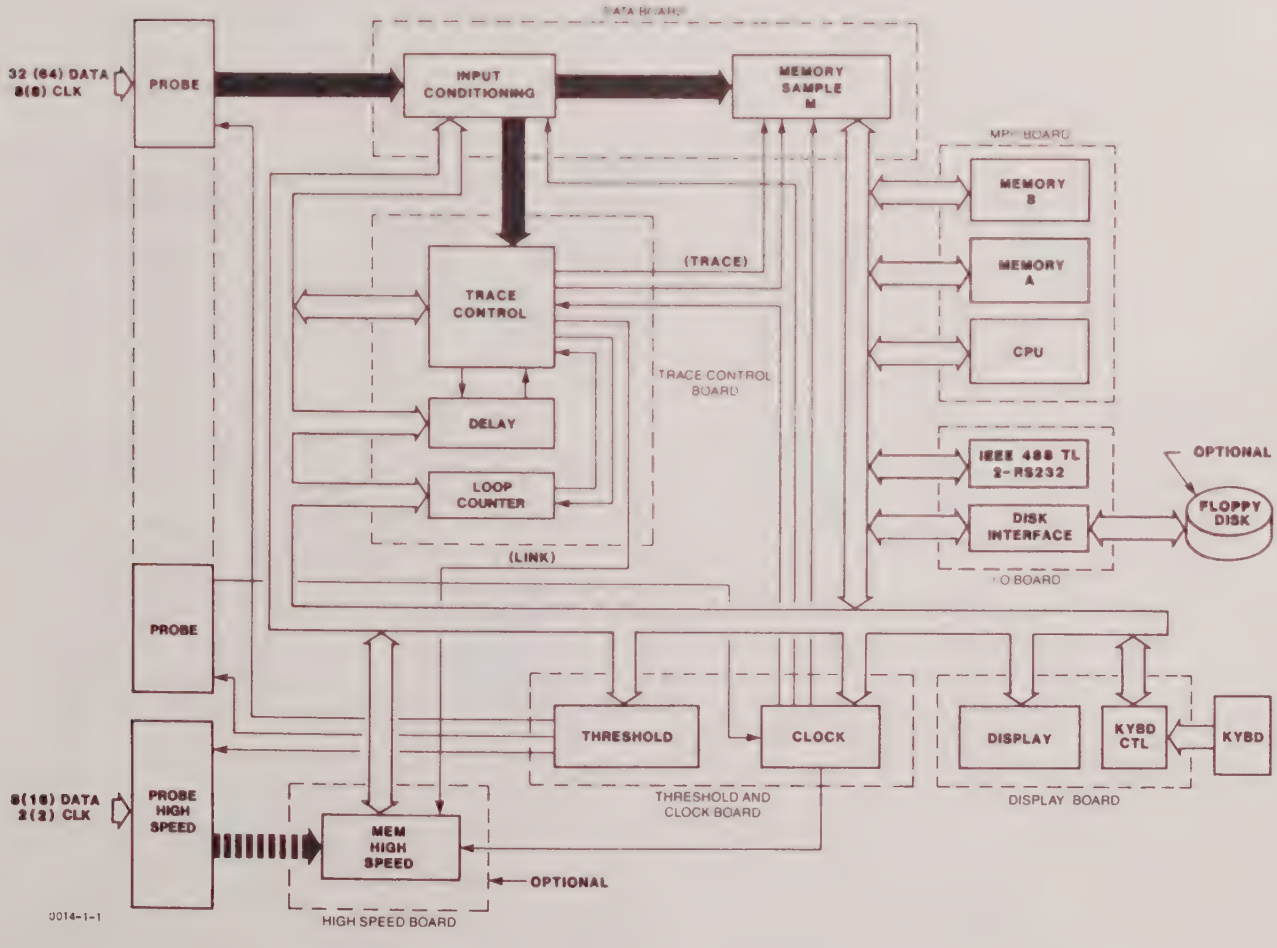


Figure 2-2. K105-D Block Diagram

SUGGESTED TEST EQUIPMENT

The following is a list of suggested test equipment for use in servicing and troubleshooting the K105-D Logic Analyzer:

Extender Boards	-Gould Part Numbers 0117-0195-01 and 0117-0135-01
Digital Multi-meter	-Fluke 8050A or equivalent
Frequency Counter	-Capable of 0.01% accuracy on ECL at 100MHz.
Oscilloscope	-Tektronix* 485 or equivalent
Logic Analyzer	-Any current production Gould logic analyzer
Pattern Generator	-Figure 2-3 provides a schematic diagram for a simple pattern generator suitable for use in the servicing of the unit.
RS-232 Wrap Back Cable	

*Tektronix is a registered trademark of Tektronix, Incorporated.

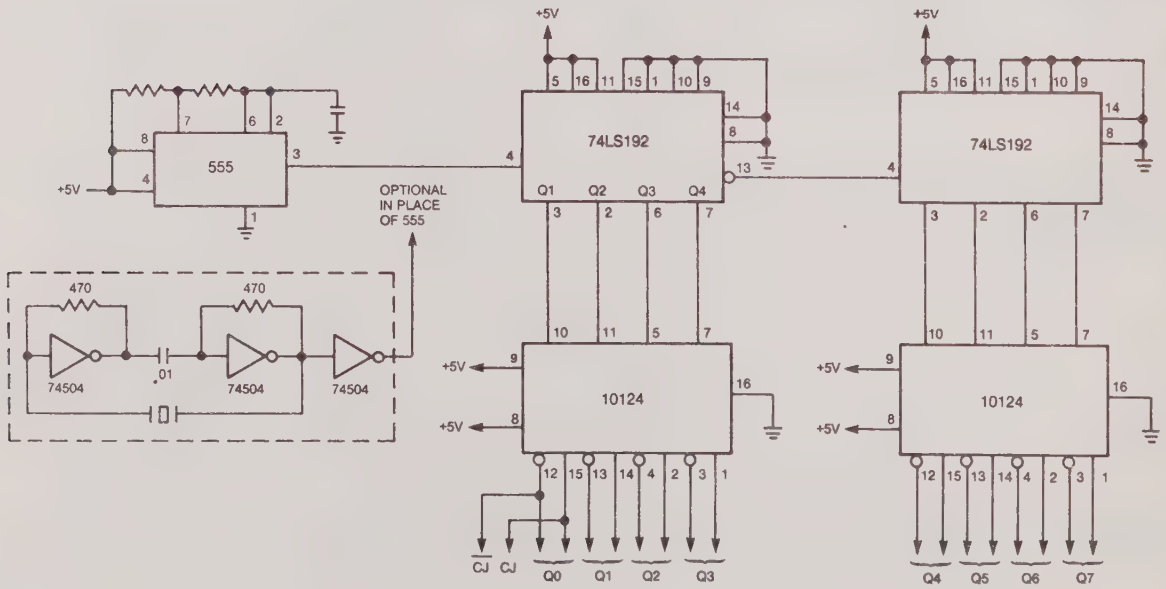


Figure 2-3. Pattern Generator Schematic

Chapter 3

CALIBRATION AND POWER-UP DIAGNOSTICS

POWER SUPPLY ADJUSTMENTS

To adjust the power supply output voltages, it is mandatory that the power supply is operating under full load. All voltage adjustments must be made with all probes connected to the unit. The following procedures describe the individual voltage adjustments and the locations on specific printed circuit boards where the voltages should be measured. All voltage adjustments shall be made on the power supply, as shown in Figure 3-1.

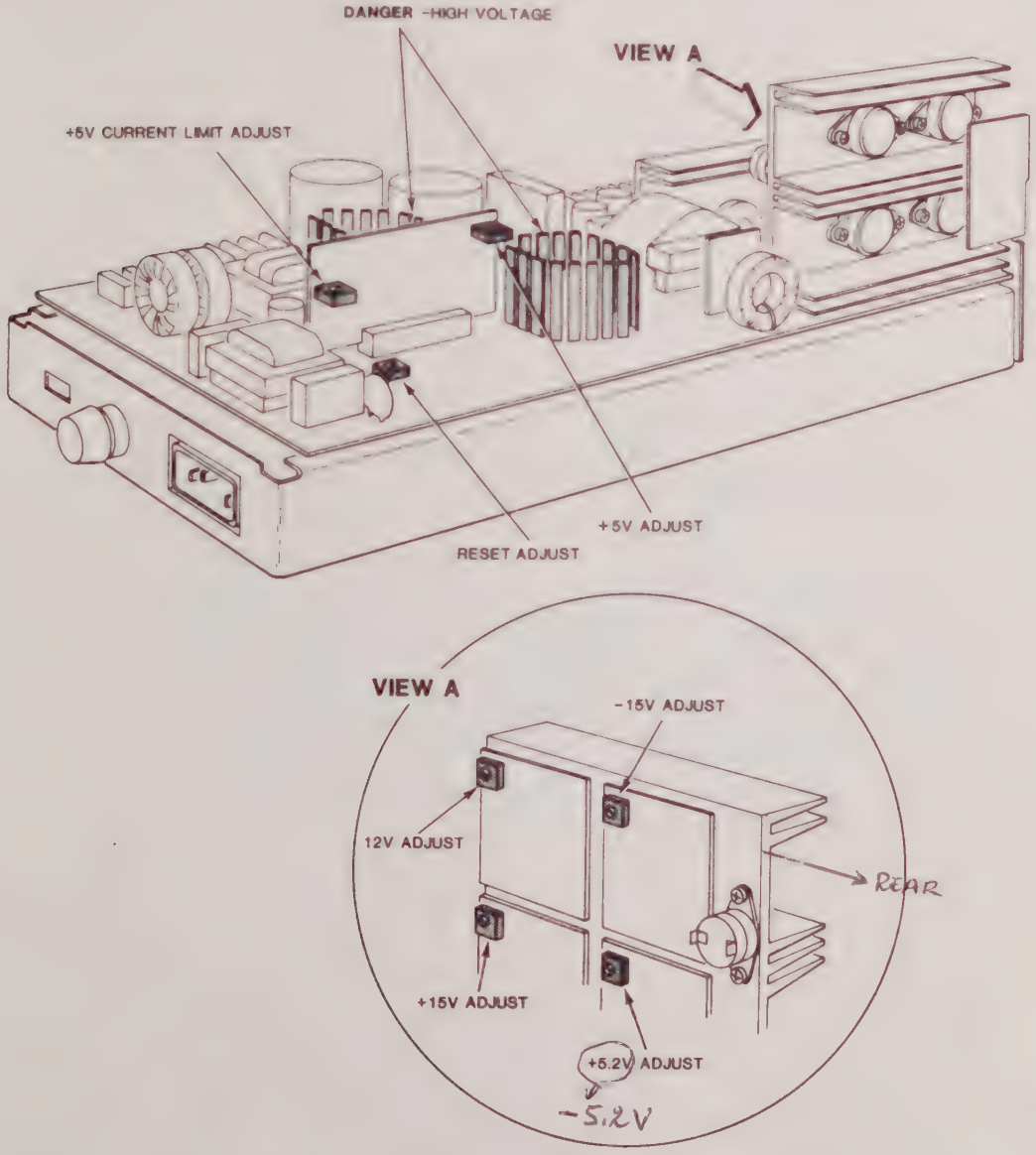


Figure 3-1. Voltage Adjustment Locations

NOTE: The RESET adjustment potentiometer is not currently functional. The +5V current limit adjustment potentiometer is factory set at approximately 40 amperes and requires no further adjustments.

+5 Volt Adjustment

To adjust the +5 volt power supply output, connect a digital voltmeter (DVM) as follows:

1. Connect the ground lead of the DVM to the ground test point at the center of the MPU printed circuit board (see Figure 3-2).

2. Connect the positive lead of the DVM to the +5 volt test point located at the end of R18 closest to device 8A on the MPU printed circuit board. (Refer to Figure ~~3-2).~~ 3-3

3. Adjust the +5 volt potentiometer to +5 volts +/- 10 millivolts.

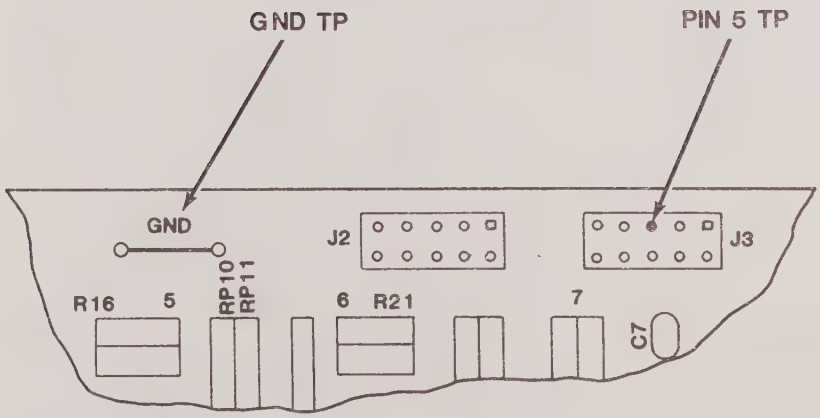


Figure 3-2. MPU Printed Circuit Board

-5.2 Volt Adjustment (USE ANOTHER METHOD ON NEXT PAGE)

To adjust the -5.2 volt power supply output, connect a DVM between the following points on the High-Speed Timing Printed Circuit Board, if installed.

1. Connect the ground lead of the DVM to the ground test point located between J1 and J2, at the top of the High-Speed timing board. (See Figure 3-3.)

2. Connect the positive lead of the DVM to the -5.2 volt test point, pin 5 of J3.

3. Adjust the -5.2 volt potentiometer on the power supply to -5.2 volts +/- 25 millivolts.

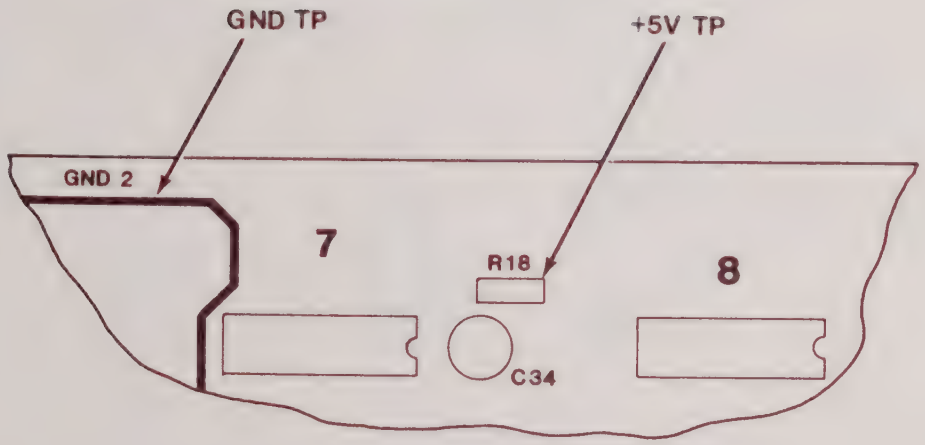


Figure 3-3. High-Speed Timing Printed Circuit Board

-5.2 Volt Adjustment (Alternate Method)

In the event that there is no High-Speed board installed in the unit, the following procedure provides alternate test points for the adjustment of the -5.2 power supply output.

1. Refering to Figure 3-4, connect the ground lead of thet DVM to the ground test point located at A1 on the Data board.

2. Connect the positive lead of the DVM to 2A, pin 8 of this same Data board.

3. Adjust the -5.2 volt potentiometer on the power supply to -5.2 volts +/- 50 millivolts.

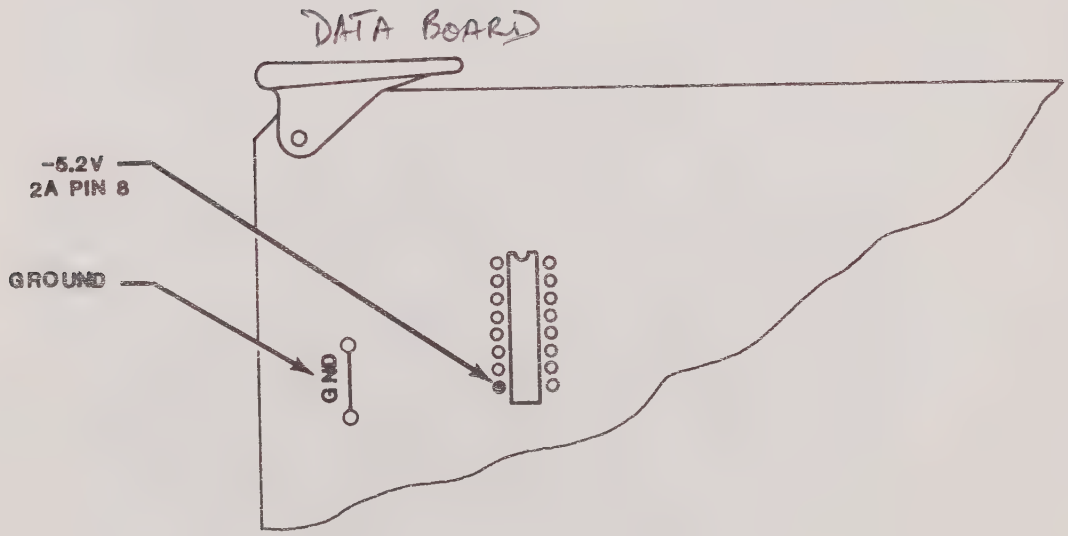


Figure 3-4. Data/Memory Printed Circuit Board

The +/- 15 volt and +12 volt adjustments are performed at their respective output terminals on the power supply. (See Figure 3-5.) NEXT page

+12 Volt Adjustment

1. Connect the ground lead of the DVM to terminal 2 of the power supply output terminal strip.
2. Connect the positive lead of the DVM to terminal 1 of the power supply.
3. Adjust the +12 volt potentiometer for +12 volts +/- 25 millivolts.

+15 Volt Adjustment

1. Connect the ground lead of the DVM to terminal 4 of the power supply.
2. Connect the positive lead of the DVM to terminal 3 of the power supply.
3. Adjust the +15 volt potentiometer for +15 volts +/- 25 millivolts.

-15 Volt Adjustment

1. Connect the ground lead of the DVM to terminal 4 of the power supply.
2. Connect the positive lead of the DVM to terminal 5 of the power supply.
3. Adjust the -15 volt potentiometer for -15 volts +/- 25 millivolts.

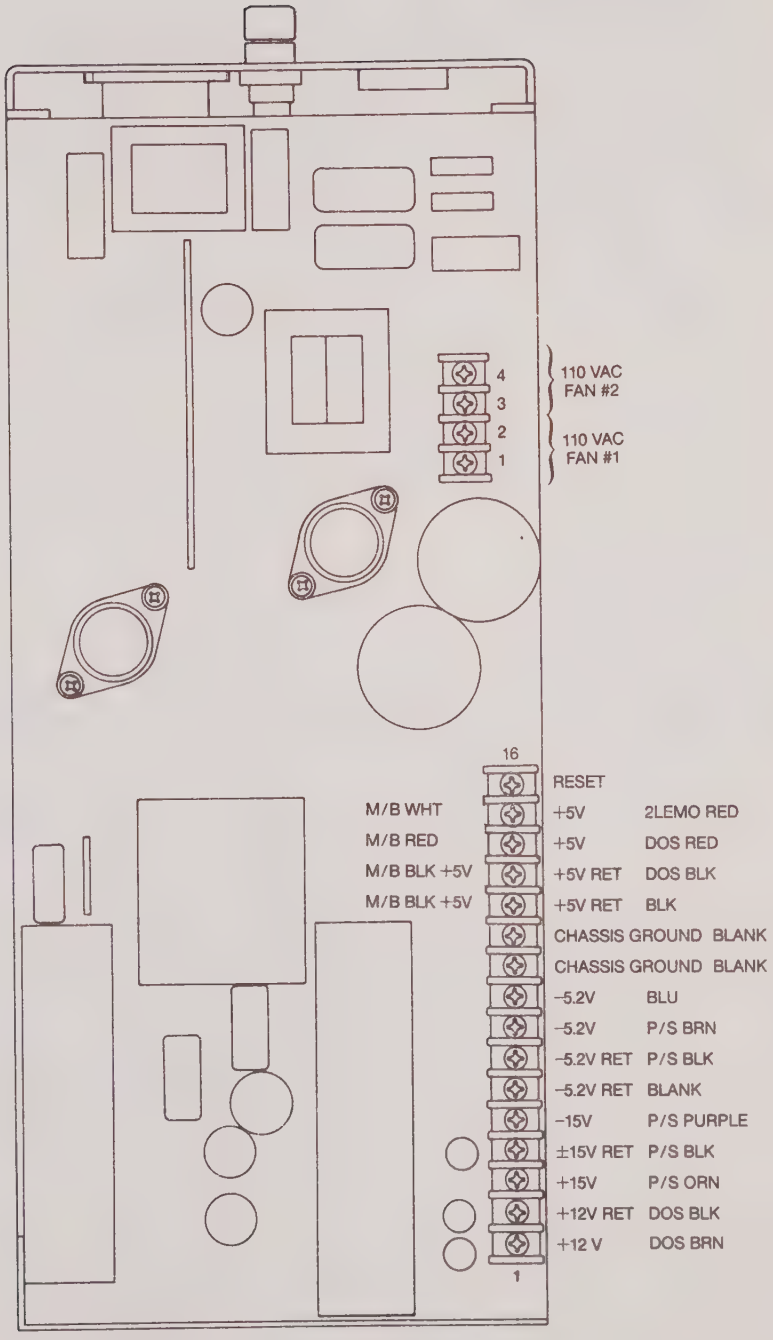


Figure 3-5. Power Supply Output Terminals

```
* * * * * * * * * * * * * * * * * * * * *
*                                         *
*                 WARNING                 *
*                                         *
* Hazardous voltages are present on the   *
* Data Display board and Cathode Ray      *
* tube.  Avoid body contact with these    *
* items.                                  *
* * * * * * * * * * * * * * * * * * * * *
```

A display calibration pattern is provided by the K105-D firmware. This pattern is accessed by depressing and holding the SHIFT key while powering up the unit. Raster adjustments are made with the Data Display board fully installed in the chassis. The technician is cautioned that the calibration controls are located near an area where high-voltages are generated for operation of the CRT. Body contact with the printed circuit board and flyback transformer should be avoided. The technician is further cautioned to use nonmetallic tools when making the raster adjustments.

Prior to attempting any height, width or linearity adjustments, the technician must first ensure the calibration pattern is centered. Centering is accomplished using the intersection point of the "X" traces as a reference point and locating the point to the center of the screen by moving and centering rings on the CRT yoke (see Figure 3-6).

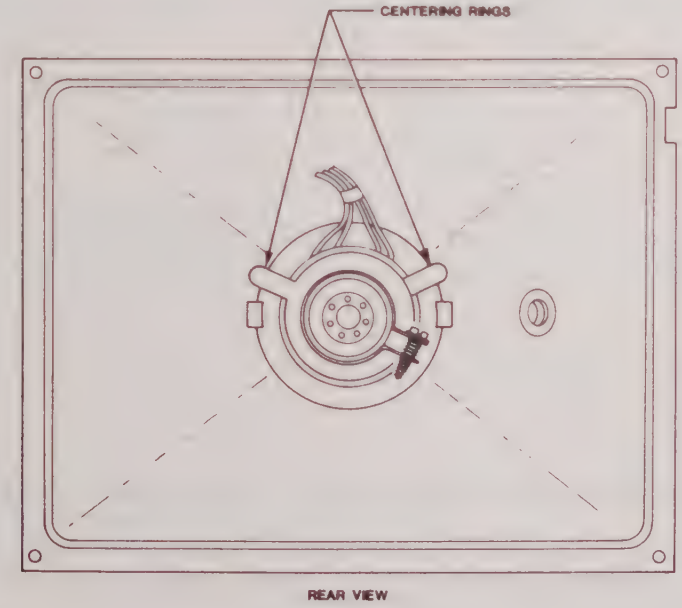


Figure 3-6. Centering Rings

Because all raster adjustments are interacting, recentering might be necessary as height, width and linearity adjustments are made. Refer to Figure 3-7.

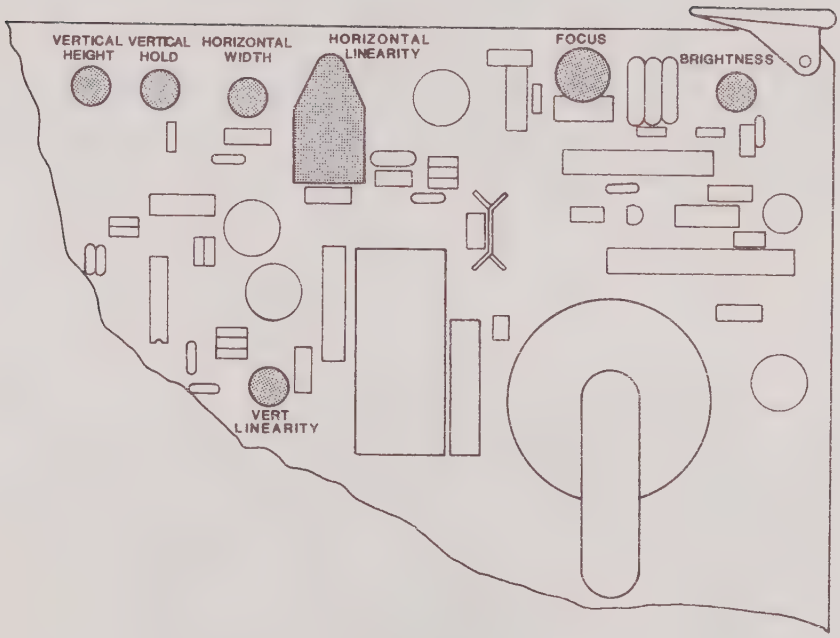


Figure 3-7. Data Display Board Adjustment Points

When it is necessary to place the Data Display board on an extender board for purposes of servicing, the user must fabricate extenders for the CRT second anode cable and the cable for the CRT base pins.

NOTE: When the user wishes to disconnect the second anode cable from the CRT, he is cautioned to discharge the high-voltage power supply capacitors by using a thin bladed screwdriver connected to ground via a clip lead and sliding the screwdriver blade under the second anode cap.

THRESHOLD/CLOCK BOARD ADJUSTMENTS

The threshold level and clock adjustment points on this board are shown in Figure 3-8. The following equipment is required to make these adjustments:

Extender Board - Gould Part Number 0117-0195
Digital Multi-meter - Fluke 8050A
Frequency Counter - Capable of 0.01% accuracy on ECL at 100 Mhz.
4.7K ohm resistor

Adjustments are made as follows:

Oscillator Adjustment

With a frequency counter at 1B pin 6, adjust C4 on the 100 MHz oscillator for 100.0 +/- .1 MHz. See Figure 3-8. Power- down the unit and reperform the adjustment procedure.

ADC Reference Adjustment (THRESHOLD BOARD J1)

a. Connect DVM reference to the board "A" gnd. (J1-4). Connect DVM input to (J1-23).

b. Adjust R21 for a DVM reading of +2.560 +/- .0005V. See Figure 3-3.

TTL Adjustment

a. Configure the K105 with one Data board.

b. Install a 4.7K ohm resistor between pins 2 and 15 of probe connector A (7-0). Connect the DVM pos. (+) lead to pin 2 and the neg. (-) lead to pin 15.

c. Make the following keyboard entry: "ARM".

d. Adjust R19 for a DVM reading of +1.4V +/- 5mV.

e. Check the other probe connector TTL levels by moving the resistor to the other probe connectors (check connectors A-D). Verify that the TTL - threshold of +1.4V +/- 25mV is present at pins 14 and 15 of the low bytes (7-0) and pin 15 of the high bytes (F-8).

NOTE: Upon power-up, the default threshold voltage selected is TTL.

ECL Adjustment

a. Return resistor to probe connector A (7-0) and connect DVM pos (+) lead to pin 2 and the DVM neg. (-) lead to pin 15.

b. Make the following keyboard entries to change all thresholds to ECL:

1. "FORMAT"
2. "CURSOR DOWN"
3. Quick-key 1 and hold until all thresholds are ECL
4. "ARM"

c. Adjust R17 for DVM reading of -1.3V +/- 5mV.

d. Check the other ECL reference levels by moving the resistor to the other input connectors (check connectors A-D). Verify the ECL threshold of -1.3V +/-25mV is present at pins 14 and 15 of the low bytes and pin 15 of the high bytes (f-8).

Variable Threshold Adjustment

a. Return resistor to probe connector A (7-0) and connect DVM pos. (+) lead to pin 2 and the DVM neg. (-) lead to pin 14.

b. Make the following keyboard entries: (already in Format screen from previous ECL adjustment).

1. "F2"
2. Hold down quick-key 2 until all thresholds read °VAR°
3. "CURSOR RIGHT"
4. "CURSOR RIGHT"
5. "0"
6. "0"
7. "ARM"

All inputs should now have VAR = 0.0V.

c. Adjust R11 for 0.00V +/- 5mV.

d. Keystroke the following entries:

1. "9"
2. "9"
3. "ARM"

e. Adjust R12 for 9.9V +/- 5mV.

f. Enter the following keyboard entries:

1. "0"
2. "0"
3. "ARM"

g. Adjust R11 for 0.00V +/- 5mV.

h. Keyboard entries: "9", "9",T", "ARM".

i. Keystroke "Cursor Left", "NEXT", "ARM"

j. Note DVM reading and adjust R12 for halfway between the actual reading and -9.90V.

k. Repeat steps c. through i., until the offset is the same for both positive and negative voltages.

l. Power-down the unit.

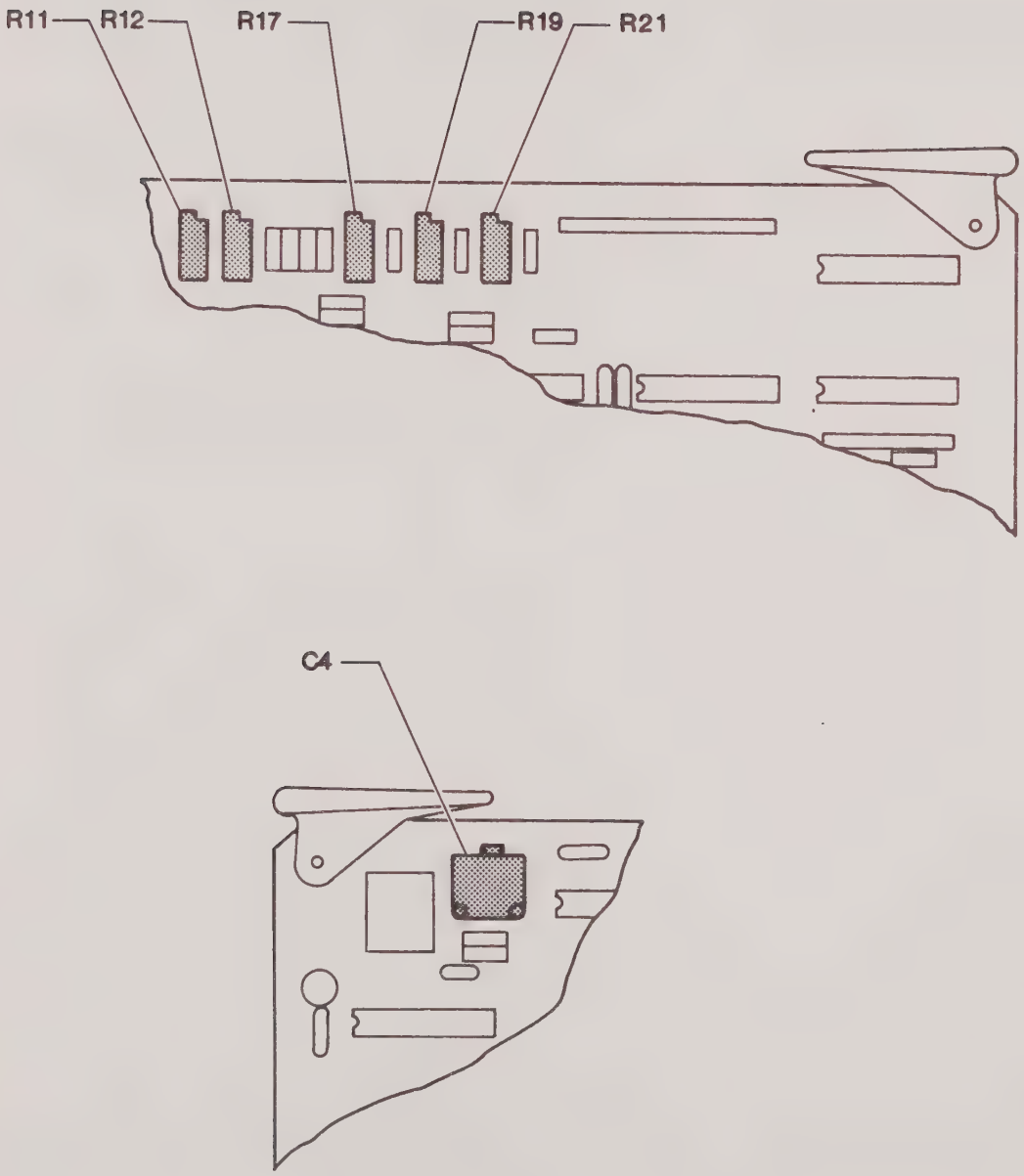


Figure 3-8. Clock and Threshold Adjustment Points

K-105 POWER-UP DIAGNOSTICS

General

Upon power-up, the K105 runs through a short series of tests. As each test begins, the name of the test is displayed on the CRT. If the test passes, the word 'PASSED' is printed after the test name. The first failure encountered in a test prints the word 'FAILED' after the name of the test, then prints a test results header on the following line and the results of the test on the line after that. Any further failures encountered in the test prints their results on successive lines. When the screen becomes full, it starts scrolling the data upwards, just as a terminal would.

The power-up diagnostics check out the microprocessor RAM and ROM, test for stuck keys, measure all system voltages, test the main channel acquisition RAM, the trace control recognition RAM and the high speed channel acquisition RAM and test for the presence of 20 millisecond timer interrupts.

Microprocessor RAM Test

This test consists of four passes:

1) Write 0000 to addresses 0000-FFFF
2) Read 0000 from addresses FFFF-0000, writing FFFF
3) Read FFFF from addresses 0000-FFFF, writing 0000

If all patterns are read back successfully, the following is displayed:

```
MICROPROCESSOR RAM TEST - PASSED

 - - - - - - - - - - - - - - - -
 = =             = =
  - - - - - - - - - - - - - - - -
```

This graphic display represents the bits in RAM, from MSB on the left to LSB on the right. Any bits in error are flagged with a bright bar between the top and bottom dotted lines.

The K105 uses a bit-mapped screen display that displays a portion of the microprocessor RAM. If any of the RAM chips are failing, vertical lines appear across the display. By using broad horizontal bars to represent RAM failures, the test results can be interpreted even if several of the RAM chips are not functioning.

Main (20 MHz) Acquisition RAM Test

The two 32-bit front-end/data boards are tested separately. Each test consists of writing 32-bit patterns consisting of a walking zero in a field of ones. The patterns are written to all 1024 locations and repeat every 9 locations. Since nine is not a power of two, address line failures should be detected by this test. If a failure is detected, the board number, the 32-bit value expected and the 32-bit value actually read are displayed. Currently, the boards are numbered 0 and 1.

Trace Control Recognition RAM Test

This routine tests the 10 RAMs on the trace control board that are used for word recognition. Three of the address lines for each RAM are connected to the trace level counter, while six or seven address lines are driven by data from the front end boards. The data lines can be read and written directly via ports EAH, ECH and EEH.

The test consists of writing a series of patterns to the RAMs while varying the level counter and changing the front end data. In all, 512 different combinations of level and front end data are used.

Ports EAH and EEH are word ports, while port ECH is a byte. If only half of the RAMs are installed (for a 32-input only system), port EEH is not tested at all, and only the lower four bits of port ECH are tested.

If a failure is detected, the error detail line shows the ports, the level number, the 64-bit data written to the front end boards, the data written to the port and the data actually read from the port.

High Speed RAM Test

The RAM for each high speed board is tested independently. A 9-byte pattern is written to the high speed RAM. The pattern is tested independently. A 9-byte pattern is written to the high speed RAM as follows: is 0FEH, 0FDH, 0FBH, 0F7H, 0EFH, 0DFH, 0BFH, 07FH, 0FFH. After 1024 writes, the read bit is set high and the data port is read 1024 times. Output from the data port is compared to the pattern written. If any byte read does not match its corresponding byte in the pattern written, the high speed RAM test fails, and the board that fails, the byte written and the byte read are displayed on the screen.

Microprocessor ROM Test

This test computes 16 bit checksums for each of the ROMs. The checksum is compared with the expected values, which are stored in the top of ROMs 15 and 16. If they do not match, the error line displays the ROM number, the expected checksum and the actual checksum. Note that a missing ROM gives a checksum of E000. The ROMs are numbered from 1 to 16. I/O ROMs are numbered I/O 1 through I/O 4.

Stuck Key Test

This test checks the keyboard matrix for stuck keys. Stuck keys are displayed below the test-failed message in a matrix that is continuously updated. When all keys are unstuck, the system proceeds to the next diagnostic.

If all keys were stuck, the following would appear:

```
KEYBOARD STUCK KEY TEST - FAILED

NX /\   > CN SH IO ED AR
PR <   \/ RF HL SP IN ST
F0 DT AB C  D  E  F  F1
CK TM MH 8  9  A  B  F2
TC GR SE 4  5  6  7  F3
AM AL CP 0  1  2  3  F4
```

Voltage Test

Voltages tested in this routine are ANALOG GROUND, +15.0 V, -15.0 V, +5.0 V, +6.2 V, -5.2 V, -6.2 V, and +5.12 V. Tolerance for analog ground has been arbitrarily set to +/- 1.0 V; tolerances for the remaining voltages have been set to +/- 10%.

1. Tests analog ground up to 100 times; if the voltage returned is not within the tolerance limit on or before test 100, returns test failed.

2. If analog ground passes, tests remaining voltages. Returns test failed if any of the voltages do not fall within acceptable limits.

For each voltage that fails, the voltage being tested, the minimum voltage limit, the maximum voltage limit and the actual voltage read are displayed on the CRT.

THEORY OF OPERATIONS

CLOCK/THRESHOLD THEORY OF OPERATIONS (0117-0055)

Overview

Figure 4-1 presents a block diagram of the Threshold/Clock board. The Threshold/Clock board is used by the K105 to decode the low speed external clocks, generate internal clocks for both the low and high speed sections, generate threshold voltages, and convert analog voltages to digital equivalents.

Address Decode Logic and Control Registers

Reference page 1 of the schematics

This function is performed by the LS27, LS10, and LS14 on the lower left-hand side of the page. If an I/O command is issued to address (2X)hex, 9G- pin 12 goes low, signifying that the Threshold/Clock board has been addressed. IC 9G further decodes the start convert and read ADC commands. ICs 8D and 9F store the data bits that determine which voltages are used for thresholds at the probes.

On page 2, the address is further decoded by 8G and 8F. The rest of the circuitry on page 2 are control registers holding the control bits. One more control register is on sheet 6 of the schematic at board location 8C.

Internal Clocks

Reference page 5 of the schematics

This section generates the internal clocks used by both the low speed and high speed sections of the K105.

All the internal clocks are derived from the 100 MHz clock circuit comprising Y1, 1B, C4, and L1. The crystal, Y1, is used in a series resonant mode. The tank circuit, L1 and C4, tunes the oscillator circuit to 100 MHz. It exhibits a low impedance shunt to off-frequency oscillations and a high impedance to 100 MHz. The output from 1B-14 is used to bias the d.c. level at 1B-13 to Vbb. Since the ECL parts are being powered by +5 volts for Vcc and 0 volts for Vee, Vbb is approximately 3.7 volts.

Counters 2B, 3A, 4A, 5A, 6A, and 7A are used as divide by 10 counters. Each counter's output is fed to the adjacent counter so that the next counter divides the original input by a factor of ten more. Thus, the first counter, 2B, divides the 100 MHz by 10 to 10 mhz. The second counter, 3A, divides the 10 MHz by 10 to 1 MHz. This continues until we get to the sixth counter, 7A, where the output frequency is 100 Hz.

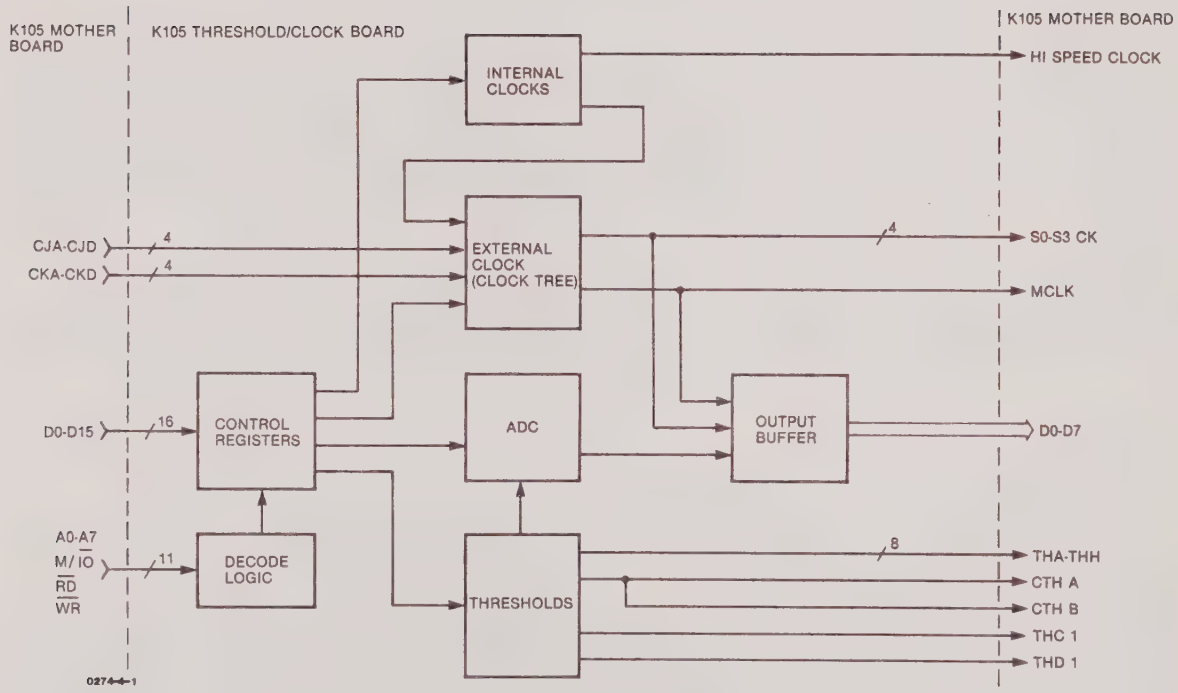


Figure 4-1. Threshold/Clock Board Block Diagram

Multiplexers 7B and 7C are used to select the frequency of interest. Counters 6B and 6C then divide the frequency by 5 and 2. The divide by 5 and 2 outputs are fed to 4B and 4C. The final selected frequencies appear at outputs 5B-6 for the low speed section and 5B-12 for the high speed section. Since the 74LS90 (6B) does not have the bandwidth to divide 100 MHz by 5 and 2, an ECL part is used. This frequency division is accomplished by 2B and 1C. The final clock output for the high speed section is at 3C-14 and 3C-15. Note that the high speed clock is driven differentially for improved noise immunity.

IC 5B, location 2c, is not used.

External Clock Decode

Reference pages 3 and 4 of the schematics

The clock tree is used to decode the external clocks per a given clock equation in the following form:

clock = (DJ*CJ*BJ*AJ) + (DK+CK+BK+AK)

The equation selected can have any of its terms deleted or negated.

There are four such independent equations and clocks. They all have identical circuits. Since the decode hardware is the same for all the clocks, only the one for S0 clock will be described. All external clocks are buffered and translated to TTL levels by 1J, 2J, 3J and 4J.

Clock decoding for S0 is done by 1H, 2H, 3H, 4H, 2D and 4D. The AND function in the clock equation is performed by 3H and 4H. The output at 4D-3 is the inverted signal of the AND term. The OR term of the CK clocks is performed by 1H and 2H. The output at 2D-3 is the inverted output of the OR term. The final decoded output is located at 4D-11 and its complement at 2D-11. These two outputs are fed into multiplexer 5D. The outputs of the other three clock equations and their complements are also fed into this multiplexer. This allows software to choose one of the eight possible selections for use as S0 CLK. There are five such multiplexers, one for each of the five clock lines used in the K105 low speed section. The lines are S0 CLK, S1 CLK, S2 CLK S3 CLK, and M CLK. These clock lines are derivatives of the original four independent clock equations.

Threshold Circuit

Reference page 1 of the schematic

The threshold circuitry is made up of three parts: the voltage reference, the digital to analog converter and the analog multiplexer.

The voltage reference is generated by using a temperature-compensated zener diode (CR3) with a zener voltage of 6.2 volts. This diode is in a feedback configuration across op amp 9B in order to produce -6.2 volts at 9B-8.

This voltage is inverted using another op amp to get +6.2 volts at 9B-14. These two voltages are required to power the analog multiplexers. The voltage reference gets its power from the +15 and -15 volts of the power supply.

The digital to analog conversion is done by the DAC 08 and an op amp at 9B. The DAC 08 uses the reference current going into pin 14 to determine its total current sinking capability at pins 4 and 2. The total current going into both pins 4 and 2 equals 255/256 times the reference current. The outputs from the register at 9D determine the current distribution to pins 4 and 2. When all outputs are high, all the current flows into pin 4 and no current flows into pin 2. When all outputs are low, all the current flows into pin 2. The reference current is controlled by potentiometer R12.

The op amp at 9B following the DAC 08 is used as a current to voltage converter. The current flowing into the DAC 08 pin 4, also flows thru R31 generating a voltage at 9B-7. This voltage is dependent on the voltage at 9B-5. When all the digital inputs to the DAC 08 are high, R12 is adjusted so that the voltage at 9B-7 is +6.35 volts. When all the inputs are low, R11 is adjusted so that the voltage at 9B-7 is -6.40 volts. This allows for an incremental voltage change of 50 mv.

The TTL and ECL thresholds are generated by using a resistor divider network. This voltage is buffered by op amps in 10B. Notice that the outputs are halved and have the required opposite polarity. The opposite polarity is required for the probes and the voltages are doubled by the buffers that follow the analog multiplexers.

The threshold voltages are tied to the inputs of eleven analog multiplexers, eight of which are for the eight data sections, one for the low speed external clocks, one for the high speed external clocks, and one for the high speed data. This allows software to select one of the three voltages (TTL, ECL, VAR) as the threshold.

The outputs of the analog muitiplexers are buffered by an op amp circuit with a gain of two. This increases the range of the DAC output.

ADC Circuit

Reference page 6 of the schematics

This circuit allows software to check the power supply and reference voltages upon power-up. The heart of the ADC circuit is the National Semiconductor ADC 1001. This device converts the difference analog voltage between its pin 6 and pin 7 into a 10-bit binary code. The code can then be read by performing an IN instruction at port number 0010 1XXX two times. The first data byte read corresponds to the most significant eight bits of the ADC data (bits 9 to 2). The second data byte read contains the least significant two bits of the ADC data (bits 1 and 0). The data read from the ADC are left-justified, high byte first. Table 4-1 provides the byte sequencing for the ADC 1001.

Table 4-1. ADC 1001 Byte Sequencing

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Because the range of the ADC 1001 is limited to ground and +5 volts, the voltage inputs need to be scaled. A resistor network consisting of RP4 scales the input voltage (V) by the following equation:

$$Vin = 2.56 + V/4$$

Vin is the voltage seen by the ADC 1001. This also allows the measurement of negative voltages.

Inputs to the ADC circuit are selected via analog multiplexers 12B, 12C, and 11B. Their outputs are isolated by a 1K resistor and then tied together and buffered by the LF356 (11C). The output of the buffer is then fed into the resistor divider for scaling. The +15 and -15 volts require extra scaling and are thus divided by 2 before going into the analog multiplexer 12B.

The voltage reference is derived from the +6.2 and -6.2 volts. It is adjusted by potentiometer R21 so that the Vref/2 input (ADC 1001 pin 9) is at +2.56 volts.

MPU Data Control

Figure 4-2 is an illustrative block diagram of the trace control board.

Reference page 2 of schematics

Data from or to the MPU bus is controlled by ICs 18A through 18D and gates 17E and and 18E. Bus addresses E0H through EFH are decoded to enable MPU data to be written or read to various ports within the trace control board. MPU data may be transferred as words (16 bits) or as bytes (upper 8 bits or lower 8 bits). As an example, if address E0H is written, pin 6 of 18E goes high, enabling buffers 13E through 15E, while pins 15 of 18C and 18D go low, causing MPU data to be stored in latch 12E.

Loading of data from the MPU may be as words or bytes for each address port with the exception of E2H. In this case, the data must be loaded as bytes. The data for address E2H low byte contains instructions to set the level counter to a specific level and the level to which to jump if a jump command occurs during the armed cycle. The data to set the counter to a specific level is applied to 11E and comparator 10E (page 3 of the schematics). When a write occurs, pin 1/15 of 11E goes low, and 11A through 11D outputs are forced into a tri-state mode. Pins 6 of 10A and 10B are forced low while pins 5 and 7 of 11D are pulled high. The write command also generates a CLK2 to set/reset flip-flops 8C and 8D. If the data to set the counter level is different from the actual counter level, pin 6 of 10E goes low, preventing data being written into 11C and 11D. This prevents data for a specific level from writing over data for a different level. If pin 3 of 10E is low (bit 2, address E0H), data is always prevented from being written into 11C and 11D, thereby allowing software to change level while leaving 11C and 11D data unchanged.

Clock Control

Reference page 2 of the schematic

IC 20E AND gates 19D, 21D, 21E, etc. form the clock control circuit. All clocks (CLK0 through CLK3) are derived from M-CLOCK when the trace control is processing object data. During the arming cycle, pin 11 of 19D is held low preventing M-CLOCK from passing through. In addition, setting pin 16 of 12E low resets the STOP and LINK latch, while setting pin 5 high allows CLK1 and CLK1' to be generated each time address E0H is written. After arming is complete, pin 5 of 12E is set low while pin 6 and 16 are set high. The first M-CLOCK (full or partial) completes the arm cycle by resetting latch 20E-B. The next M-CLOCK generates CLK0, CLK1, and CLK1' and resets latch 20E-A while CLK2, -CLK2', and CLK3 are suppressed. This allows object data to be latched into 1E through 8E while preventing a decision from occurring based on object data stored from the previous arming or armed cycles. Subsequent M-CLOCK's generate CLK0 through CLK3.

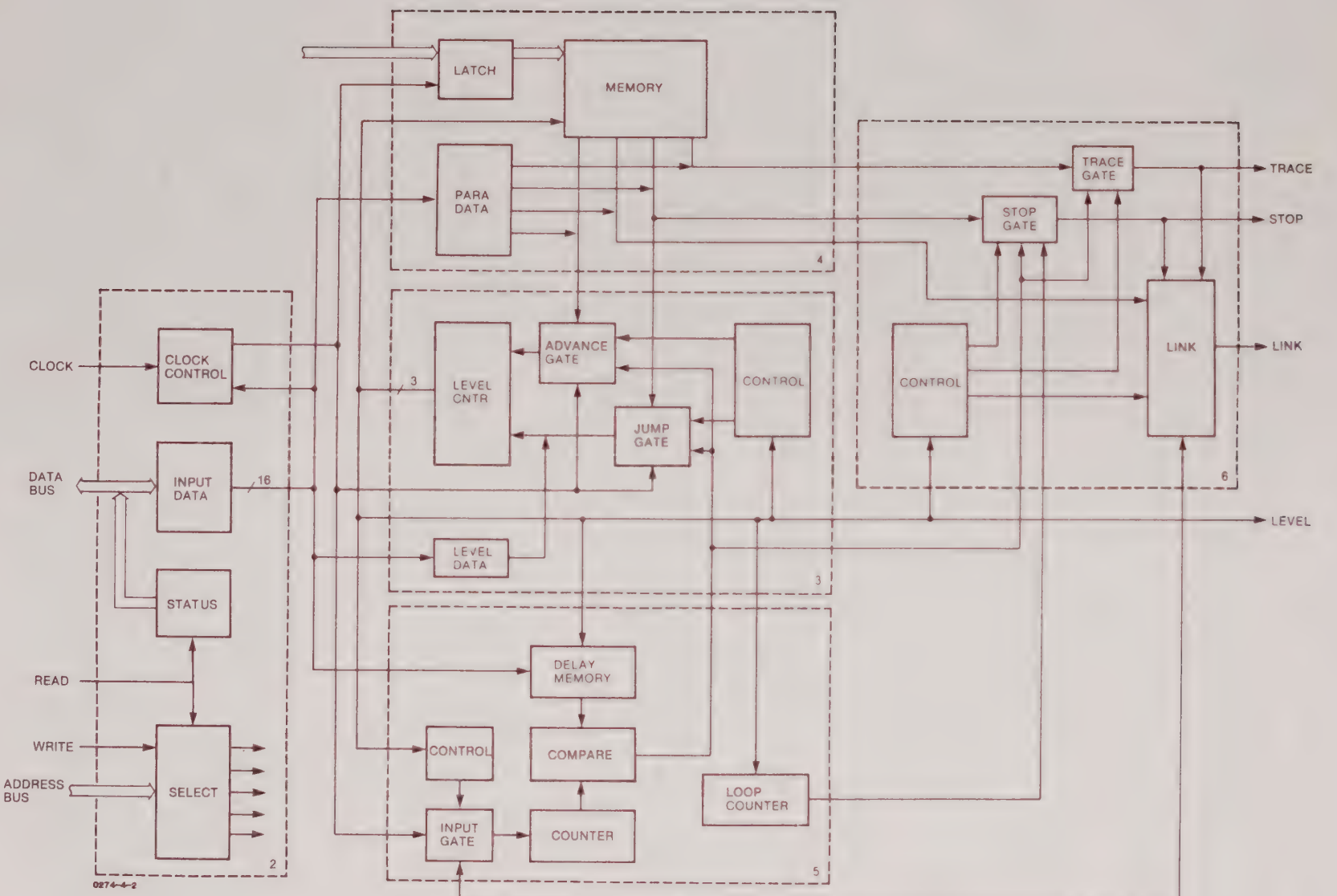


Figure 4-2. Trace Control Board Block Diagram

M-Clock

Reference page 2 of the schematics

M-CLOCK is also preprocessed by gates 21E, 17E, and 19D to form a clock pulse between 10ns and 15ns wide at pin 8 of 19D. This prevents the level counter from slewing for M-CLOCK pulse widths greater than 35ns.

RAM Recognition

Reference page 4 of the schematics

2C and D through 6C and D form the recognition memory. Object data is clocked into latches 1E through 8E by CLK1 and CLK1'. This data along with the three bits from the level counter (pins 15, 16, and 17 on each RAM) form an address for each RAM. During the arming cycle the MPU generates this address by processing user specified addresses through the data board while storing recognition data at each address. The recognition data is written into or read back from the RAMs through bidirectional buffers 1B through 5B. During the armed cycle, object data from the users' system along with the three bits from the level counter now form the address for each RAM. For object data to be recognized, a high must be stored in each RAM at the formed address. This recognized data enables the specific gates (1C, 1D, 7C, or 7D) which control the functions stop, trace, jump, and advance.

If the system uses a single 32 input board, pin 8 on RAMs 3C, 3D, 4D, 6C, and 6D is held high forcing them into the tri-state mode. A pullup on each of the tri-state outputs allows each control function to be enabled by RAMs 2C, 2D, 4C, 5C, and 5D, exclusively.

Level Counter

Reference page 3 of the schematics

The level counter is a three bit state counter made from three flip-flops, 8C and half of 8D. The counter operates in two modes: incremental advance, and direct set/reset or jump. The counter output controls the address of each of the twelve 74F189 RAMs and forms part of the address for the data recognition RAMs. The 74F189 RAMs contain data stored during the arming cycle, to control various functions at each level.

The clock input for each flip-flop is tied to pin 8 of 7B. Two of the inputs of 7B are connected to 10D and 10C which together form an EXCLUSIVE OR function. The inputs to 10D and 10C are controlled by the ADVANCE function, 7D, from the RAM recognition section and data from level control RAM 11D. The other two inputs to 7B are CLK2 and pin 8 of 10C which in turn is driven by manual advance, 20D, and DELAY, 10B. If pin 8 of 10C is assumed to be high, then a high at pin 7 of 11D and a low at pin 9 of 7D (advance if true) allows the level counter to increment on the next occurrence of CLK2. If, however, a low is present at pin 7 of 11D then a high at pin 9 of 7D (advance if not true) allows the level counter to increment on the next occurrence of CLK2.

Gates 7A, 8A, and 8B along with 10D and 10C form an EXCLUSIVE OR function for the jump mode of operation. In addition, the data stored in 11C and 11D determine which level the counter jumps to on the next jump command. If pin 6 of 10A is assumed to be low then a high at pin 5 of 11D and a low at pin 9 of 7C (jump if true) allows the counter to change to the level stored in 11C and 11D on the next occurrence of CLK2. If, however, a low is present at pin 5 of 11D then a low at pin 9 of 7C (jump if not true) allows the counter to change to the level stored in 11C and 11D on the next occurrence of CLK2. It should be noted that the counter advances or jumps at the occurrence of CLK2; however, since the jump command drives the set/reset inputs of each flip-flop, the jump command takes priority over the advance command.

In both modes the outputs from pins 6 of 10A and 10B are assumed to be low. The section on the DELAY COUNTER details the operation of these IC's.

Delay Counter (With Inhibit)

Reference page 5 of the schematics

The delay counter is composed of counters 17A through 17D, comparators 16A through 16D, RAMs 15A through 15D and gates 13B and 13C. Pin 11 of 12D selects if the counter increments by clocks or advance events for a specific level. Part of 10D and 13B resets the counter any time a level change occurs. The data for a specific number of counts is stored in RAMs 15A through 15D for each level during the arming cycle. The counters 17A through 17D increment each clock or advance event. The output of the comparators, pins 5, 6, and 7 of 16A, indicate if the number of clocks or advance events counted is greater than, equal to, or less than the value of the number stored in the RAMs. Gate 13B combines the output of the comparator to generate less than or equal to, greater than or equal to, or not equal to functions. These six functions are then applied to multiplexers 10A, 10B, 21A and 21B which in turn control each of the four commands jump, advance, trace, and stop.

Each multiplexer has its input, pins 1 through 4 and 12 through 15, selected by the data for each level stored in RAM (11A, 11B, 20A, and 20B). Each multiplexer has in addition to the six delay functions, a fixed high and a fixed low thereby generating no delay or infinite delay, respectively.

Inhibit

Reference pages 3 and 5 of schematics

The inhibit circuit consists of gates 12A, flip-flop 13A, and associated components. The circuit is necessary to prevent the DELAY COUNTER from miscounting at clock rates greater than 17MHz. When the rate of CLK0 is less than 15 MHz, the voltage across C88 reaches a value of at least 1.5 volts before being reset to zero. The leading edge of CLK0 now sets pin 5, 12, and 10 of 13A to a low which in turn forces pin 9 of 13A high. Pin 3 of 13C now holds pins 7 of 10A and 10B low enabling normal operation of both multiplexers (inhibit defeated). When the rate of CLK0 is greater than 15 MHz, the voltage across C88 reaches a value of less than 1.5 volts before being reset to zero. The leading edge of CLK0 now sets pins 5, 12, and 10 of 13A high. If pin 12 of

10D goes low (level change), CLK2' now resets 13A forcing pin 9 low which in turn forces pins 6 and 7 of 10A and 10B high. This condition prevents an advance or jump from occurring at the next clock. Pin 12 of 10D now goes high, CLK2 sets pin 9 of 13A high restoring normal operation of both multiplexers.

Delay Counter

Reference page 5 of the schematics

The delay counter is composed of counters 16A through 16D, RAMs 15A through 15D, flip-flop 17B, and gates 9C, 13B, 13C, 17A, and 17C. Pin 11 of 12D determines if the counter decrements by clocks or by advance events for a specific level. Part of 12A resets the counter each time a level change occurs. For each level, the data for a specific number of counts is stored in RAMs 15Athrough 15D during the arming cycle. The counters, 16A through 16D, decrement each clock or advance event. The output of 9C pin 8, 17A pin 8, and 16A pin 13 indicate if the number of clocks or advance events counted is greater than, equal to, or less than, respectively, the value of the number stored in the RAMs. Gate 13B combines the output of the comparator to generate less than or equal to, greater than or equal to, or not equal to functions. The output of 17B pin 5 generates the less than or equal to function. These six functions are then applied to multiplexers 10A, 10B, 21A, and 21B which in turn control each of the four commands: jump, advance, trace, and stop.

A level change (or arming cycle) forces pin 13 of 17B to go low. Pins 11 of 16A through 16D are also forced low, transferring in data from RAMs 15A through 15D. CLK0 forces pin 9 of 17B high, which in turn forces pins 11 of 16A through 16D high. A clock or event is applied, through 17A, to pin 14 of 16A through 16D, which decrements the counter by one. The pulse applied to pin 14 occurs at least three gate delays after pin 11 is forced high, thereby ensuring the counter decrements immediately after a level change. Each clock or event decrements the counter until a zero is reached, at which time pin 13 of 16A goes low, pin 8 of 17A high, and pin 2 of 17B low. Pin 5 of 17A is also forced low which prevents clock or event pulses from further decrementing the counter. The next clock or event to occur forces pin 5 of 17B and pin 8 of 17A low, and pin 8 of 9C high. The counter remains in this state until the next level change.

Each multiplexer has its input (pins 1 through 4, and 12 through 15) selected by the data, for each level, stored in RAMs 11A, 11B, 20A, and 20B. Each multiplexer has, in addition to the six delay functions, a fixed high and a fixed low, thereby generating no delay or infinite delay, respectively.

Loop Counter

Reference page 5 of the schematics

The loop counter consists of counters 14A through 14C, latch 14D, comparator 13D, and gates 12B and part of 12C. The LOOP COUNTER determines the level to be counted and the number of times to be counted. When the terminal count is attained, trace operation is unconditionally stopped. Each time a new level

is entered, pin 6 of 13D goes high if the level equals the data stored in 14D.

This in turn decrements counters 14A through 14C. When the count equals zero, pin 8 of 12B goes high forcing pin 6 of 13D and pin 13 of 14A low, which in turn stops trace operation. The LOOP COUNTER remains in this condition until a new arming cycle occurs.

Link

Reference page 6 of the schematics

The link circuit consists of multiplexer 21C, half of flip-flop 22D, and gates 17E and 19B. The multiplexer has its inputs (pins 1 through 4, and 12 through 15) selected by the data for each level stored in RAM 20C. If an input pin on 21C goes low and is selected at a specified level, then pin 6 is forced high. Pin 9 of 22D is then latched high. The circuit remains in this state until a new arming cycle occurs. The first link event to occur generates the link signal and succeeding link events are ignored.

Stop

Reference page 6 of the schematics

The stop function consists of part of gates 19B, 19C, 22A, 22B, and 22C, and half of flip-flop 22D. Gates 22A, 22B, and 22C form an EXCLUSIVE OR function. The inputs to 22A, and 22B are controlled by the STP function (1C, page 4 of the schematics) from the RAM recognition section and data from control RAM 20B. The input to pin 9 of 22C is the Delay function detailed in the section on the delay counter. If pin 6 of 21B is assumed to be low, then a high at pin 7 of 20B and a low at pin 9 of 1C (stop if true) causes the stop latch to be set on the next occurrence of CLK2; additionally, if a low is present at pin 7 of 20B, then a high at pin 9 of 1C (stop if not true) also causes the stop latch to be set on the next occurrence of CLK2.

The stop latch, 22D, may also be set if pin 4 goes low. If pin 5 of 20C is low for a specific level and an ADVANCE occurs, or if pin 13 of 14A (LOOP COUNTER) goes low, or if pin 12 of 12E (KEY STOP) goes low, an unconditional stop results.

The stop latch remains in a set condition until a new arming cycle occurs.

Trace

Reference pages 4 and 6 of the schematics

The trace or record function consists of parts of gates 21E, 22A, 22B, and 22C. Gates 22A, 22B, and 22C form an EXCLUSIVE OR function. The inputs to 22A and 22B are controlled by the TRACE function, 1D, from the RAM recognition section and data from RAM 20A. The input to pin 1 of 22C is the DELAY function detailed in the section on the delay counter. If pin 6 of 21A is assumed to be low, then a high at pin 5 of 20A and a low at pin 9 of 1D (trace if true) causes a record pulse to occur (pin 3 of 21E) on the next

occurrence of CLK2; additionally, if a low is present at pin 5 of 20A, then a

high at pin 9 of 1D (trace if not true) causes a record pulse to occur (pin 3 of 21E) on the next occurrence of CLK2.

The following charts refer to activity on the system address/data bus; for a given address placed on the bus, the corresponding data appears on the bus.

SETUP DATA / DIAGNOSTIC CLOCK

ADDRESS = XXE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								HME	MCE	DCE	M>A	STP	JDE	ARM	MAD

Bit 0 = Manual ADvance: A high advances the state level counter one level with the next M-clock. A low must be entered to clear the register before the next high can cause another advance.

Bit 1 = ARM: A low starts the arm cycle. The M-clock must be disabled (Bit 6).

Bit 2 = Jump Data Enable: A low prevents jump data, bits 3 thru 7 of address E2, from being written but allows 0 through 2 to change the state level counter.

Bit 3 = STоP: A low stops all operation.

Bit 4 = M>A: A high enables the transfer of data from the sample memory to the A memory, starting with the next D-clock or M-clock.

Bit 5 = D-Clock Enable: A high enables the diagnostic clock. A D-clock is generated at the same time the bit is set and each time E0 is written until the bit is set to a low. This bit must be set low at least one command before MCE (bit 6) is set to a high.

Bit 6 = M-Clock Enable: A high enables the M-clock. During the arm cycle, the M-clock must be disabled. When data for the arm cycle is loaded, the MCE bit is then set to a high and the next M-clock pulse completes the arm cycle. This bit must not be set high in the same command as DCE (bit 5) is set to a low.

Bit 7 = High Memory Enable: A low enables the high (channels 32 thru 63) portion of the trace comparator memory.

ADDRESS = XXE2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JGD	JED	JLD	JEN	AGD	AED	ALD	AEN	JP2	JP1	JP0	AWT	JWT	PC2	PC1	PC0

NOTE: Data for this address MUST be entered as two separate bytes. Low byte first, high byte second.

Bit 0-2 Program Controller 0 - 2: Sets the program controller to any level, absolutely (level 0 = 000, level 1 = 001, level 7 = 111). Program controller does not change level unless new command is entered OR circuit is armed and a jump or advance event occurs.

Bit 3 Jump When True: A low causes a jump to occur if event is true. A high causes a jump to occur if event is not true.

Bit 4 Advance When True: A low causes an advance to occur if event is true. A high causes an advance to occur if event is not true.

Bit 5-7 Jump Program Control 0 - 2: Data to instruct the program controller which level to jump to if a jump event occurs.

NOTE: Bits 3 thru 7 can only be loaded if bit 2, address E0, is set high.

Bit 8 Advance ENable: A low enables the advance event. To be used with bit 4, as follows:

B8	B4	
0	0	Advance if true
0	1	Advance if not true
1	0	Advance never
1	1	Advance always

NOTE: Advance never, using B8 and B4, is not to be used if delay on advance event is used. If advance never is required then bits 9 - 11, below, are to be used.

Bit 9-11 Delay Advance: Data to set conditions for delaying the advance event.

B11	B10	B9	
0	0	0	Disable advance delay.
0	0	1	Advance if event occurs when less than programmed count.
0	1	0	Advance if event occurs when equal to programmed count.
1	0	0	Advance if event occurs when greater than programmed count.
0	1	1	Advance if event occurs when less than or equal to programmed count.
1	1	0	Advance if event occurs when greater than or equal to programmed count.
1	0	1	Advance if event occurs when not equal programmed count.
1	1	1	Advance never.

Bit 12 Jump ENable: A low enables the jump event to be used with bit 3, as follows:

B12	B3	
0	0	Jump if true
0	1	Jump if not true
1	0	Jump never
1	1	Jump always

Bit 13-15 Delay Jump: To set conditions for delaying the jump event.

B15	B14	B13	
0	0	0	Disable jump delay.
0	0	1	Jump if event occurs when less than programmed count.
0	1	0	Jump if event occurs when equal to programmed count.
1	0	0	Jump if event occurs when greater than programmed count.
0	1	1	Jump if event occurs when less than or equal to programmed count.
1	1	0	Jump if event occurs when greater than or equal to programmed count.
1	0	1	Jump if event occurs when not equal programmed count.
1	1	1	Jump never.

DELAY / LINK DATA

ADDRESS = XXE4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TGD	TED	TLD	TWT	SGD	SED	SLD	SWT	LBC	LBB	LBA	LSP	DCA	LGT	TEN	SEN

Bit 0 Stop ENable: A low enables the stop event to be used with bit 8, as follows:

B0	B8	
0	0	Stop if true
0	1	Stop if not true
1	0	Stop never
1	1	Stop always

Bit 1 Trace ENable: A low enables the trace event to be used with bit 12, as follows:

B1	B12	
0	0	Trace if true
0	1	Trace if not true
1	0	Trace never
1	1	Trace always

Bit 2 Level GaTe: A low enables the output gate during a specified level.

Bit 3 Delay Advance Clock: A low enables the delay counter to count each advance event detected. See note regarding advance enable.

Bit 4 Level StoP: A high causes an unconditional, undelayed stop to occur if an advance occurs at the selected state level.

Bits 5-7 Link Bit A thru C: Data to set link event

B7	B6	B5	
0	0	0	Link never.
0	0	1	Link when level first entered.
0	1	0	Link when exiting level.
0	1	1	Link on jump.
1	0	0	Link on advance.
1	0	1	Link on trace.
1	1	0	Link on stop.
1	1	1	Link never.

NOTE: Link on jump, advance, trace, or stop includes delay or "not" functions if so programmed.

Bit 8 Stop When True: A low causes a stop to occur if event is true. A high causes a stop to occur if event is not true.

Bit 9-11 Delay Stop: Data to set conditions for delaying the stop event.

B11	B10	B9	
0	0	0	Disable stop delay.
0	0	1	Stop if event occurs when less than programmed count.
0	1	0	Stop if event occurs when equal to programmed count.
1	0	0	Stop if event occurs when greater than programmed count.
0	1	1	Stop if event occurs when less than or equal to programmed count.
1	1	0	Stop if event occurs when greater than or equal to programmed count.
1	0	1	Stop if event occurs when not equal programmed count.
1	1	1	Stop never.

Bit 12 Trace When True: A low causes a trace to occur if event is true. A high causes a trace to occur if event is not true.

Bit 13-15 Delay Trace: Data to set conditions for delaying the trace event.

B15	B14	B13	
0	0	0	Disable trace delay.
0	0	1	Trace if event occurs when less than programmed count.
0	1	0	Trace if event occurs when equal to programmed count.
1	0	0	Trace if event occurs when greater than programmed count.
0	1	1	Trace if event occurs when less than or equal to programmed count.
1	1	0	Trace if event occurs when greater than or equal to programmed count.
1	0	1	Trace if event occurs when not equal programmed count.
1	1	1	Trace never.

DELAY COUNTER DATA

ADDRESS = XXE6

Bit 0-15 Delay Count: Data to set the specified count for the delay counter.
Bit 0 = LSB (low = true)
Bit 15 = MSB (low = true)

LOOP COUNTER

ADDRESS = XXE8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB	<	-	-	-	-	-	-	-	-	->	LSB	LB2	LB1	LB0	LEC

Bit 0 Enable Loop Counter: A high enables the loop counter.

Bit 1-3 Level Bit 0 - 2: Binary data that equals level to be counted.

Bit 4-15 Loop Count: Data to set the specified count for the loop counter.
Bit 4 = LSB (high = true)
Bit 15 = MSB (high = true)

PARAMETER DATA

All parameter data is arranged in four bit groups in the order jump, advance, trace, and stop. A high at any location equals a true condition for any state level for the specified trace input data. Data may be written or read using the same address.

ADDRESS = XXEA

Bit 0-3	Trace input Data 0 (TD0) thru Trace input Data 5 (TD5)
Bit 4-7	TD6 thru TD12
Bit 8-11	TD13 thru TD18
Bit 12-15	TD19 thru TD25

ADDRESS = XXEC

Bit 0-3	TD26 thru TD31
Bit 4-7	TD58 thru TD63

ADDRESS = XXEE

Bit 0-3	TD32 thru TD37
Bit 4-7	TD38 thru TD44
Bit 8-11	TD45 thru TD50
Bit 12-15	TD51 thru TD57

STATUS

ADDRESS = XXE0 (Reads status of trace control)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								f MX	S TP	L KD	L C0	Q 13	Q 12	Q 11	A RM

Bit 0 ARMed: A low indicates trace control is armed. Armed becomes true when the first word of data is stored and becomes false one clock after a stop.

Bit 1-3 Q11 - Q13: Binary data indicating program control level.

Bit 4 Loop Counter equals 0: A low indicates loop counter reached specified count.

Bit 5 LinKeD: A high indicates a link event has occurred.

Bit 6 SToPped: A low indicates a stop has occurred.

Bit 7 f MaX: A high indicates the inhibit circuit is active.

K105-D TRACE CONTROL SOFTWARE SPECIFICATION SUMMARY

		ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETUP DATA / DIAGNOSTIC CLOCK	W	XXE0									HME	MCE	DCE	M>A	STP	JDE	ARM	MAD
LEVEL CONTROL	W	XXE2	JGD	JED	JLD	JEN	AGD	AED	ALD	AEN	JP2	JP1	JP0	AWT	JWT	PC2	PC1	PC0
DELAY/LINK DATA	W	XXE4	TGD	TED	TLD	TWT	SGD	SED	SLD	SWT	LBC	LBB	LBA	LSP	DCA	LGT	TEN	SEN
DELAY COUNTER DATA	W	XXE6	MSB	<- - - - - - - - - - - - - - -							- - - - - - - - - - - - - - ->							LSB
LOOP COUNTER DATA	W	XXE6	MSB	<- - - - - - - - - - - - - - -							- - - - ->			LSB	LB2	LB1	LB0	ELC
LOOP COUNTER	W	XXE8	MSB	<- - - - - - - - - - - - - - -							- - - - ->			LSB	LB2	LB1	LB0	ELC
PARAMETER DATA	W/R	XXEA	S	T	A	J	S	T	A	J	S	T	A	J	S	T	A	J
PARAMETER DATA	W/R	XXEC									S	T	A	J	S	T	A	J
PARAMETER DATA	W/R	XXEE	S	T	A	J	S	T	A	J	S	T	A	J	S	T	A	J
STATUS	R	XXE0									fMX	STP	LKS	LC0	Q13	Q12	Q11	ARM

MPU Data Control

Figure 4-3 provides an illustrative block diagram of the Data/Memory board.

Reference page 2 of the schematics

Data from or to the MPU bus is controlled by IC 19B, gate 18A, and parts of gates 18B, 19A, 19C, 19D, and 19E. Bus addresses C0H through C6H (for the lower 32 data inputs) and addresses D0H through D6H (for the upper 32 data inputs) are decoded to enable MPU data to be written or read to various ports within the data board. MPU data may be transferred as words (16 bits) or as bytes (upper 8 bits or lower 8 bits). As an example, if address C0H is read, pins 4 and 12 of 19B go low enabling buffers 3C and 7C. Data stored in RAMs 2B, 3B, 6B, and 7B is transferred to the MPU.

Data is written with address C0H. This causes pin 8 of 18A to go high which in turn latches MPU data into 18D. When pin 8 of 18A goes low, data on pins 12, 15, 16, and 19 of 18D is latched into each respective gate array: 1D, 5D, 9D, and 13D (page 3 of the schematics).

Clock Control

Reference page 2 of the schematics

Gates 17A and parts of 18B and 19A form the clock control circuit. When the system is armed, pin 5 of 17A and 19A go high, and a record pulse stores user data into RAMs 2B, 3B, 6B, etc. by advancing counters 5A, 9A, and 13A (page 4 of the schematics).

Data Processing (Gate Arrays)

Reference page 3 of the schematics

User data is first processed by ECL to TTL converters 2A, 3A, 6A, and 7A. Data is then delayed by 1C, 4C, 5C, and 8C for 25ns, after which it is processed by gate arrays 1D, 5D, 9D, and 13D. Data is pipelined through the gate arrays using clocks applied to pins 28, 29, and 34. MCLK, pin 29, places data on the TD outputs. Two MCLKs later, the same data appears on the PD outputs. The TD outputs are sent to and processed by the Trace Control circuit, which in turn determines the PD data to be stored in RAMs 2B, 3B, 6B, etc. Trace control requires two MCLK's between TD and PD data.

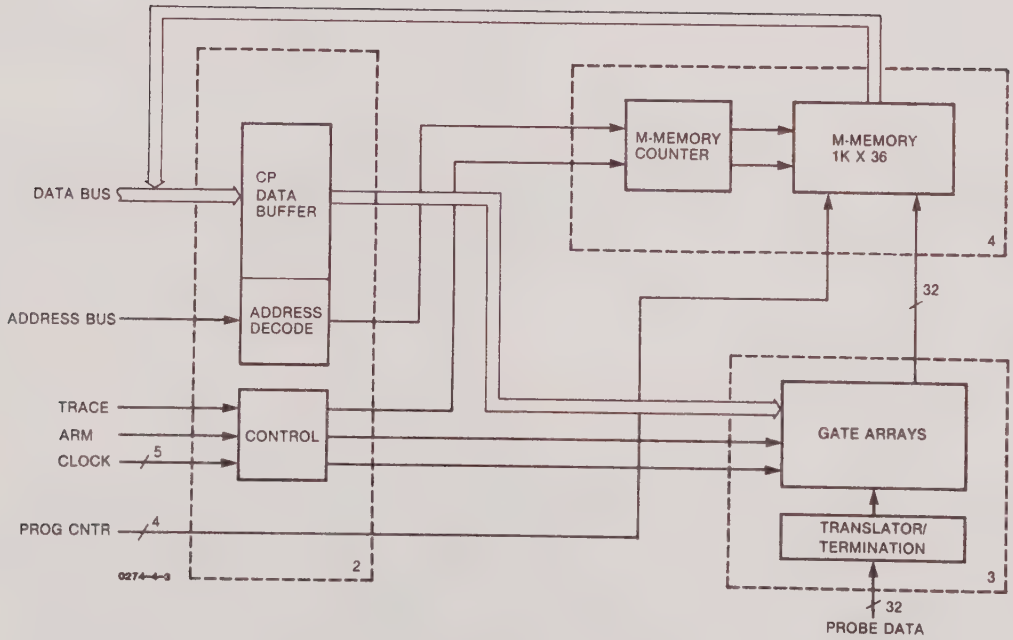


Figure 4-3. Data/Memory Board Block Diagram

Data RAMs

Reference page 4 of the schematics

Data to be stored in RAMs 2B, 3B, 6B, etc. is buffered by gates 2C, 6C, etc. When a data word is to be stored, trace control sends a RECORD pulse to the data board which in turn increments counters 5A, 9A, and 13A once for each record pulse. In addition, the same RECORD pulse causes pin 8 of all of the RAMs to go high (deselecting each RAM) for the duration of the pulse. This prevents data from being randomly stored while the RAM address lines are changing. Data is read from each RAM through buffers 3C, 7C, etc.

The following chart refers to activity on the system address/data bus; for a given address placed on the bus, the corresponding data appears on the bus.

DATA/MEMORY SOFTWARE SPECIFICATIONS

INPUT DATA

ADDRESS = XXC0 (XXD0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								CPDT4	CPDT3	CPDT2	CPDT1	SDEMX2	SDEMX1	SDTIN	CPSL

Bit 0 — Central Processor SeLect: A high allows CP data to be passed thru the data path in place of external data. In addition, if memory counter is advanced (read address XXC4), CP data is stored in memory.

Bit 1 — Select Data IN: A high allows external data to be passed through the data path.

Bit 2 — Select DEMultiplex 1: A high selects the demultiplex mode for channels A and B.

Bit 3 — Select DEMultiplex 2: A high selects the demultiplex mode for channels C and D.

Bits 4-7 — Central Processor DaTa 1 - 4: CP data, in byte serial form, to be passed through the data path in place of external data according to the following:

Bit 4 = 11 10 9 8 3 2 1 0
Bit 5 = 15 14 13 12 7 6 5 4
Bit 6 = 27 26 25 24 19 18 17 16
Bit 7 = 31 30 29 28 23 22 21 20

OUTPUT DATA

ADDRESS = XXC(V)

V = 0 Data: Channels 0 thru 15

V = 2 Data: Channels 16 thru 31

V = 4 Data: BD0 = Program counter 0
BD1 = Program counter 1
BD2 = Program counter 2
BD3 = Link true
BD4 = MSB of memory counter
BD5 = Zero if armed
BD6 = Zero if recording
BD7 = Zero if board is installed

V = 6 (LO BYTE ONLY) CPCLK: CP clock used in place of M-Clock, S0, S1, S2, and S3 during the arm cycle.

V = 6 (HI BYTE ONLY) CTRCLK: Counter clock is used to increment the internal memory counter (M>A must be enabled from trace control).

When the system is configured for 64 data channels, 32 thru 64 become address XXD0. All other specifications are adjusted accordingly.

Address Decoder

Figure 4-4 presents an illustrative block diagram of the High Speed board.

Reference page 1 of the schematics

The address decoder looks at the system address base and enables the board upon receipt of address 8X and 9X (hex) or AX and BX (hex). The two address pairs depend on how many high speed boards are installed in the system. If the system is configured for eight timing inputs, the address AX and BX are decoded. With the addition of the second eight timing inputs, the address group 8X and 9X configure the second high speed board. When the proper address is decoded, the data that is resident on the data bus is latched into a set of registers (page 2 of the schematics). These registers hold the data that subsequently configure the board to perform a specific task.

Level Shifters And Output Control

Reference page 1 of the schematics.

The level shifters (13E, 14E, 15E and 16E) convert the +ECL signal to TTL signals to be compatible with the data bus. The level shifters perform the inverting function where necessary. These are also gated so that the proper group of signals can be read onto the bus when commanded to do so by the CPU. The two groups of data available for transportation to the CPU are 7 status bits and 8 data bits.

Set Up Latches

Reference page 2 of the schematics

The set up latches store the data states that are used to set up the high speed board. These commands are decoded from the data bus when the board has been properly addressed.

Level Shifters

Reference page 3 of the schematics

The purpose of level shifters is to change the -ECL signals from the probes to +ECL levels as used on the boards. This consists of the 4039 differential amplifiers that convert the signals to approximately the level required, followed by a differential line receiver 10216 to set up the proper ECL levels for the data and clocks.

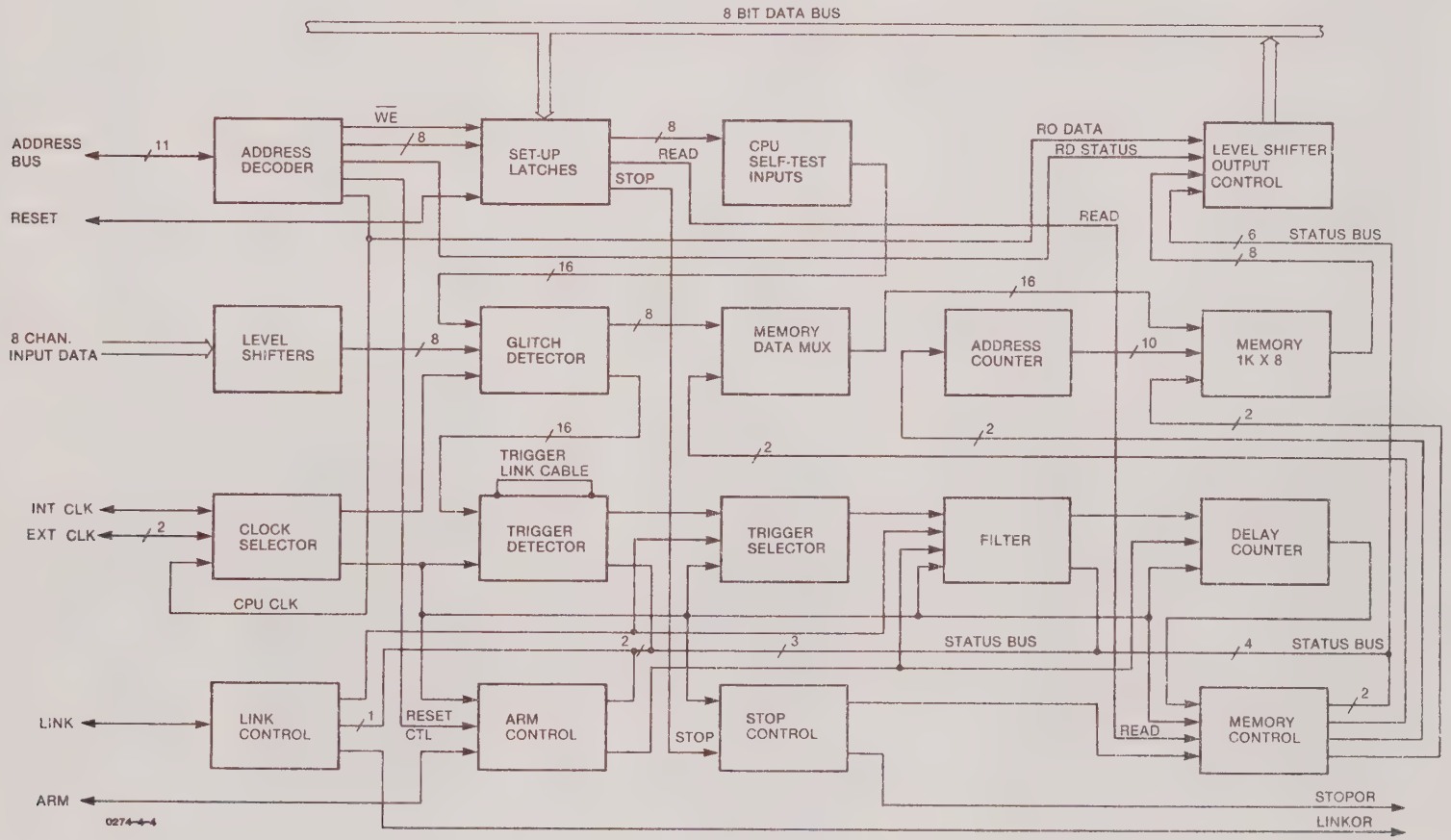


Figure 4-4. High Speed Board Block Diagram

Clock Selector

Reference page 4 of the schematics

The clock selector is used to select the clock that operates the system when making a recording. The selection consists of Internal Clock, External HJ Clock using the rising or falling edge, External HK clock using the rising or falling edge and the CPU clock derived from the Read command. The clock selected is then buffered and distributed through the board.

CPU Self Test Inputs

Reference page 5 of the schematics

The CPU self test inputs are a series of AND - NOR (5E through 8E) gates that either set or reset the D flip-flops just prior to the trigger tree decoder so that a defined data word can be inserted into the data path to check the trigger detector, the filter, the counter and the memory system, as well as the readback circuitry.

Glitch Detector

Reference page 5 of the schematics

The purpose of the glitch detector is to find pulses whose duration is less than one clock cycle. The glitch detector finds pulses as small as 5 ns duration. When not set in the glitch detection mode, it merely clocks data through to the trigger tree. In the glitch mode, the input gates are set up in such a way that the presence of a glitch causes the first D-flip/flop to be set or reset and hold that state until the data is clocked through. When the clock passes the glitch through the D-flip/flop, it also causes the gate structure to reverse and reset the glitch on the next cycle. The data is passed through the detector in the normal manner.

Trigger Detector

Reference page 5 of the schematics

The trigger detector is a group of gates that are programmed to detect the presence of a particular word that exists in the data stream. When the word is detected, a pulse is generated. The pulse duration is equivalent to the number of clock cycles that the word existed in the data stream.

The trigger circuit has an external trigger cable whose purpose is to link together the triggers of two high speed boards. This is necessary when operating in the 16 input mode and the required trigger exists across the 16 inputs of the data stream.

Trigger Selector

Reference page 5 of the schematics

The trigger selector determines whether the system is to trigger on the presence of a trigger, the absence of a trigger or not use a trigger word at all. The trigger selector network is not activated until the trigger is not present, after which it looks for the trigger. Should a trigger be present when the circuit is armed, the trigger selector ignores this trigger and waits for another occurrence of the trigger before actually triggering the system.

Memory Data Demultiplexer

Reference page 6 of the schematics

The memory data demultiplexers (7C, 7D, 8C and 8D) demultiplex the data into two streams so that the data can be loaded into two different memories on alternate clock cycles. This is done so that the 100 MHz clock rate does not exceed the writing speed of the memories used.

Filter

Reference page 6 of the schematics

The filter (19C) is a four bit counter that counts the number of clock cycles in which the trigger word has occurred before actually triggering the system. The count can be any number of events from 1 to 15. The counter is reset after the trigger word goes away and waits for the reoccurrence of another similar trigger. This mode is available in the event that the system desires to copy the data only after a specific number of trigger events have occurred.

Delay Counter

Reference page 6 of the schematics

The delay counter (15B through 18B) is used to count the number of clocks or events from the trigger word before terminating a recording. This is a 16-bit counter capable of counting from 1 to 65535 clocks or events. In the case where events are being counted, the recording ends 500 clock cycles after the last counted event. This is done to locate the last recorded event at the center of the recording.

Link Control

Reference page 6 of the schematics

The link control (20C) determines whether the high speed board is linked to the normal channels or if it is to operate independently. The link control also has provisions to guarantee that when 16 inputs are being used, both boards link simultaneously. This is necessary to prevent a 1 clock skew between the upper and lower eight inputs.

Arm Control

Reference page 6 of the schematics

The arm control (18A, 19A and 20A) arms the high speed board from either the TRACE CONTROL or the CPU boards. The arm control also has provision for purging the old data in the system prior to arming so as to preclude any false trigger from starting the system. This is done by delaying the arming signal for 5 clock cycles so any residual data has been purged.

The arm control also provides the necessary controls for simultaneously arming two high speed boards (16 channels) from a single command from the CPU when being used in the High Speed only mode.

Stop Control

Reference page 6 of the schematics

The stop control (16A) terminates a recording on command from the CPU. It is also structured so that a stop command issued to one board will effectively stop both boards when the system is operating in the 16 channel mode. This guarantees that the high speed recording terminates without data skew.

Memory Control

Reference page 6 of the schematics

The memory control consists of dual synchronous divide by two counters (13B, 14C, and 14D). The purpose of the counter is to generate the write pulses and the memory address clock. These signals are two phase clocks used to control the two ranks of memory. The write pulse circuitry is also provided with a write pulse inhibit circuit so that the memory is not rewritten during the read cycle. The memory control also has circuitry to assure that the write pulse and the address clock are properly phased.

Address Counter

Reference page 7 of the schematics

The address counter is a dual counter that creates a binary address sequence for the memories. The two address generators are used so that each memory rank is addressed at the proper time. Since this is a dual rank memory loading scheme, the loading of each memory half is done on alternate cycles of the clock. The address generators are clocked on alternating cycles of the memory clock. The memory clock is half the frequency of the data clock.

Memory 1K By 8-Bits

Reference page 7 of the schematics

The memory consists of eight type 10422 memories. These are 256 X 4-bit ICs and are configured in four groups of 256 X 8. Two of the four groups are loaded alternately for 512 X 8 data samples, then the second two groups are loaded alternately for another 512 X 8 data samples. The memory system is continuous and loads data in alternating blocks until stopped.

I/O BOARD HARDWARE THEORY OF OPERATION
(0117-0075)

Overview

Figure 4-5 provides a block diagram of the I/O board. Communication between the board and the Logic Analyzer is done through the motherboard. Connectors on the top of the board are used for communication to the Disk Drive, RS-232C ports, and the IEEE-488 Buss. The circuitry on the board consists of buffers in/out, logic to convert the 16 bit data bus of the logic analyzer to an 8-bit data bus on the card, some Random Access Memory (RAM), Read Only Memory (ROM), a Direct Memory Access (DMA) controller, a floppy disk controller, an IEEE-488 Talker/Listener function, 2 Universal Synchronous/Asynchronous Receiver/Transmitters (USART), and a timer/baud rate generator.

Board Access

Reference page 1 of the schematics

The board has three access spaces: I/O, status, and Memory. The I/O space is defined by the contents of the ROM in location 13D. It decodes the total I/O space between 00 and 7F (Hex) of which 31 (of 128) addresses are actually used. The 31 addresses are further decoded into seven chip selects (location 7C). The status space is nearly identically decoded by the ROM in location 12D and the demultiplexer in location 8C. The status space may always be accessed, but the I/O space must only be accessed when the board is not doing DMA. The memory space may reside anywhere in the 00000 to FFFFF range (4K Byte Blocks) and is decoded by the ROM in location 17B and the demultiplexer in 18B. All of the space on the board is byte addressable, and the memory is also word (16-bit) addressable. Even address bytes are buffered through location 10D while odd bytes are buffered at location 11.5D and if necessary multiplexed from the upper to lower data buss at location 11D. Addresses are buffered at locations 13C, 14C and 14D. Control Lines are buffered through 5D, 6D and 9D.

On Board Clocks

Reference page 4 of the schematics

The board runs on the 8 MHz clock from the motherboard. Several chips use the 8 MHz directly. Location 4C is used to divide to 4 MHz, 2 MHz and 500 KHz. It is also divided by 13 (location 5C) to 1.625 microseconds which is then divided down by the counter/timer chip in location 4B to generate the baud rates for the USARTs (5B and 6B). 8 MHz is also used to generate the Phase Lock Loop X 16 clock which is either 8 MHz or 4 MHz, depending on whether double or single density floppy disks are being written to. The floppy disk also requires a 250 nanosecond write pulse (7B and 6C) at 500 KHz or 250 KHz, again depending on density.

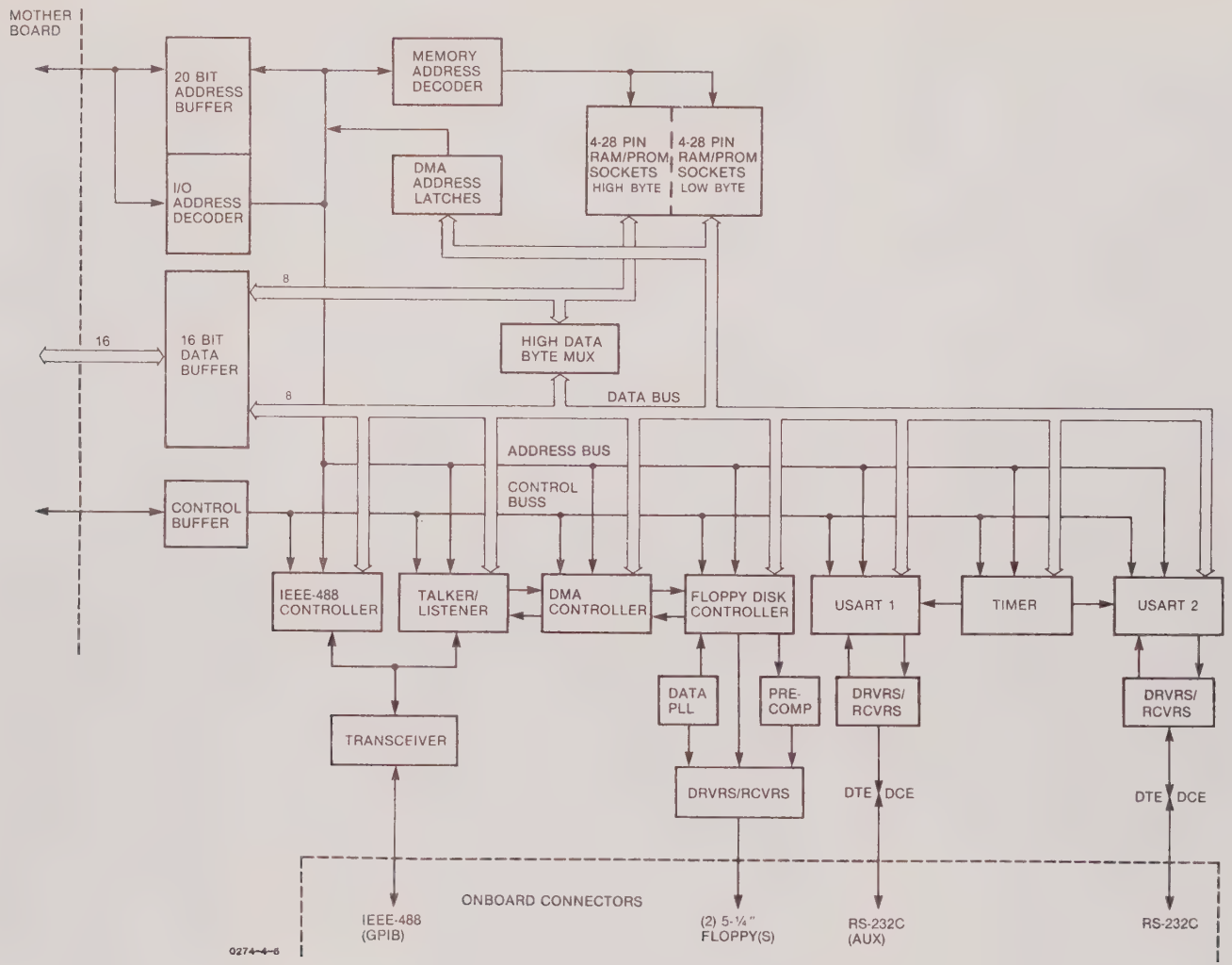


Figure 4-5. I/O Board Block Diagram

Direct Memory Access

Reference page 4 of the schematics

Location 13B is the DMA chip. The primary users of the DMA chip are the IEEE-4888 Talker/Listener chip and the floppy disk controller. In either of these cases, the off-card microprocessor must setup the board for DMA and then initiate. Once DMA is initiated, the on-card I/O space must not be accessed or a malfunction may occur. DMA may be terminated by writing the BUSRQ bit of the status space (locations 10C and 12C) and then confirmed by reading the IDLE bit (locations 9C and 11C). DMA is initiated by the DRQ (DMA Request) signal whereupon the DMA chip sends out a HLDRQ (hold request) and normally immediately receives HLDAK (hold acknowledge). The HLDAK is then sent back to the floppy disk controller as DAK (DMA acknowledge). Between HLDAK and DAK the DMA chip loaded an address on the address bus, read data from the floppy disk controller onto the data bus, and wrote it into memory (or read from memory and wrote to FDC).

Floppy Disk Controller

Reference page 5 of the schematics

Locations 3C, 1C, 2C, 1B, 2B, 3B, 1A, 2A, 1D, 2D, 3D and 4D are associated with the floppy disk controller. 1D, 2D and 4D are called the Data Separator and/or Phase Lock Loop since they do in fact lock onto the data stream being read from the floppy disk and look for data present (1s) or absent (0s) and separate that data from the clock. Chip locations 1C and 2C are used for precompensation or postcompensation (writing slightly early or late) which on double track (96 tracks per inch) floppies is necessary to avoid smearing of closely packed bits.

Universal Synchronous/Asynchronous Receiver/Transmitters

Reference page 6 of the schematics

Locations 5B and 6B along with 4A, 5A, 6A and 7A are used for RS-232 type communication. The transmit/receive bit rates are set by the timer in location 4B. The bit rate clock is usually set at 16 times the actual rate at which data is being transmitted, or in the case of an external clock exactly at the data rate. Plus and minus 15 volt line drivers are used to take the signals to the outside world.

IEEE-488 Talker/Listener

Reference page 7 of the schematics

Locations 17A, 16A and 15A are the IEEE-488 bus function. Location 18A is wired for the bus controller function but, presently is not supported with either hardware or software.

MPU BOARD THEORY OF OPERATION (0114-0186)

Overview

The MPU Board operation is controlled by an 8086 microprocessor running at 4 MHz clock rate. The circuitry on the MPU Board consists of an 8086 microprocessor, address registers, data transceivers, random access memory (RAM), read only memory (ROM), memory controller and I/O decoder. This board provides control functions for display, display setups, memory transfer, memory functions, memory compares and keyboard. Figure 4-6 is a block diagram of the MPU board.

Microprocessor

Reference page 1 of the schematics

The 8086 microprocessor (location 10L) used on the MPU Board is running at a 4 MHz clock rate in the minimum mode configuration. The 8086 microprocessor outputs a 20-bit memory address. Data is accessed as 16-bit words, subdivided into a low-order byte and a high-order byte. The low-order 16 address bus lines (AD0 to AD15) are multiplexed with the 16-bit data bus. Byte High Enable signal (BHE) is used to identify the high-order byte, while AD0 identifies the low-order byte.

Initialization or startup is accomplished with activation (HIGH) of the MPU RESET pin (location 8B) for more than four clock cycles. The 8086 microprocessor terminates operations on the high-going edge of the MPU RESET and remains dormant as long as MPU RESET is HIGH. The low-going edge of MPU RESET triggers an internal reset sequence of approximately 10 clock cycles, during which time no other operations should occur.

Non-maskable interrupt request (NMI) is initiated when external logic inputs a low-to-high transition at the NMI pin by power-up signal (PUP) at locations 11B and 11M. A non-maskable interrupt has lower priority than a software interrupt, but higher priority than a maskable interrupt. A maskable interrupt request is generated when external logic inputs a HIGH level at the INTR pin. The 8086 microprocessor responds by generating INTA for interrupt acknowledge cycle.

HOLD and HLDA are standard hold request/acknowledge signals. When external logic inputs HOLD high, the 8086 microprocessor enters a hold state upon completing the current instruction's execution; the 8086 microprocessor acknowledges the hold state by outputting HLDA high. Location 11M is the buffer for the INTR, INTA, and HLDA.

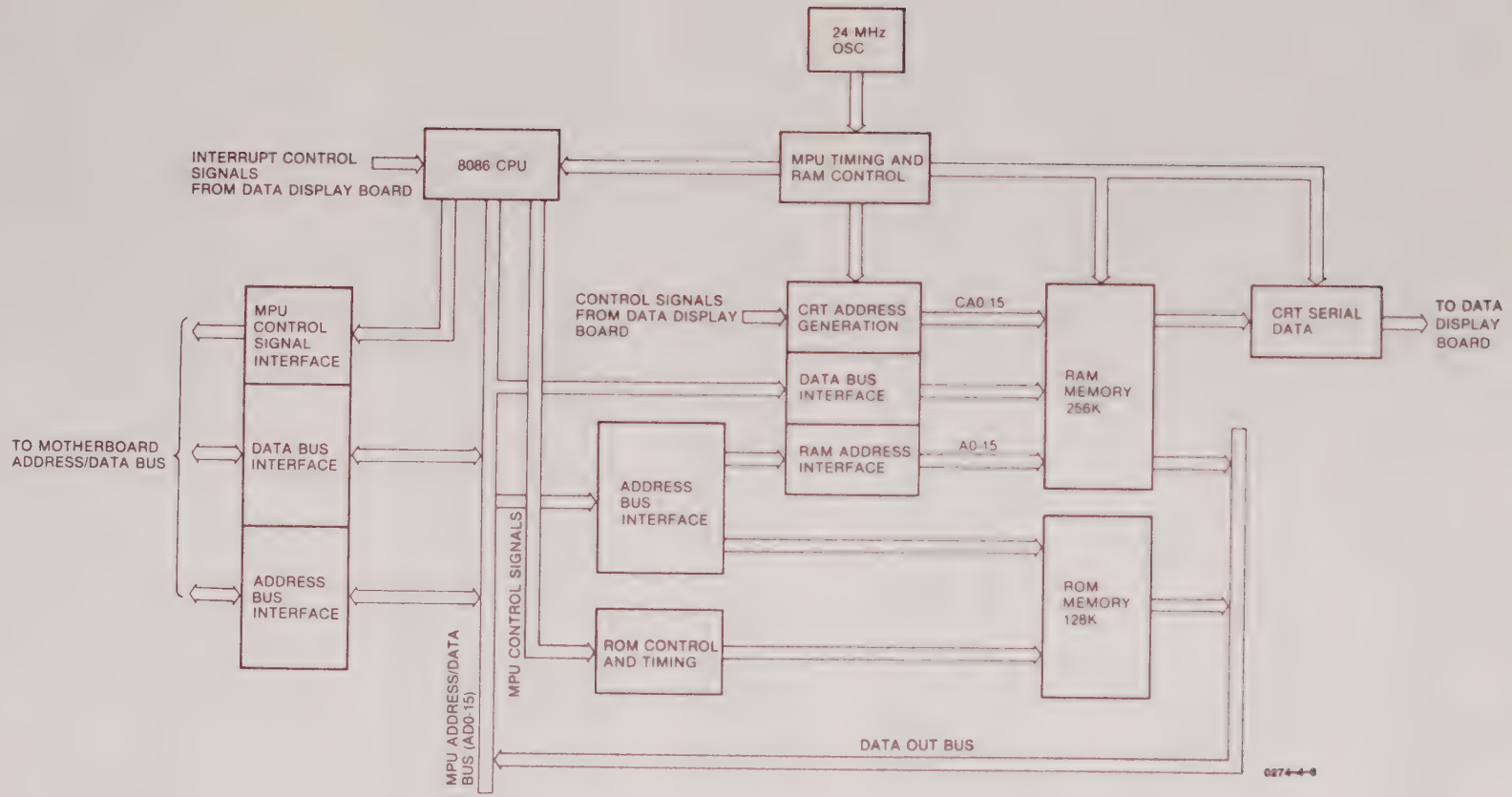


Figure 4-6. MPU Board Block Diagram

Address Registers And Data Transceivers

Reference page 1 of the schematics

The 8086 microprocessor uses a multiplexed bus for address and data transfers. The MPU Board demultiplexes the 8086 bus into two buses. One bus controls all information to the ROM and the RAM which is contained on locations 1A to 1H, 2A to 2H, 4A to 4H and 6A to 6H. The other bus interfaces with other boards in the K105-D. Locations 9K, 10K and 11K are buffers for 20 memory address lines (A0 to A19) and BHE. Locations 9M, 10M and 11L are buffers for 20 address lines and BHE to boards other than the MPU. The transceivers for the data lines are located at locations 7M and 8M. Locations 7K, 7L, 8K and 8L are wired for PROM's and buffers for temporary test only. The 8086 loads addresses into the address registers by using the Address Latch Enable signal (ALE) and then transmits (WR) the data, to or receives (RD) the data from, the address in the register.

Memory

Reference pages 2 and 5 of the schematics

The 8086 memory space is organized into 16 segments of 64K bytes of external memory space. Segment E and F (Hex) are the 128K bytes of ROM which contains the operating software. Segment 0 and 1 (Hex) contain the 128K bytes of dynamic RAM.

The ROM segment, locations 1A to 1H and 2A to 2H, uses sixteen 8K X 8 memories arranged into 8 sections of 8K words each. Locations 3J and 3K (page 4 of the schematics) are ROM chip select decoders. Data output is read from ROM through a buffer at location 3L for high-byte data and at location 3M for low-byte data.

The RAM segment, locations 4A to 4H and 6A to 6H, is made up of thirty-two 64K X 1 dynamic RAMs providing 128K words (256K bytes). Data is input into the RAM, through the buffer at location 4J for high-byte data and at location 6J for low-byte data via RAM WRITE DATA EN. Data output is read from RAM through the latch buffer at location 4K for high-byte data and at location 6K for low-byte data via MPU LATCH ENABLE and EN RAM READ. CRT Data is read out into buffer registers at locations 6L and 4L and then shifted out at an 8 MHz clock rate to the DATA DISPLAY Board by shift registers at locations 6M and 4M.

Memory Controller

Reference page 3 of the schematics

The memory timing and the clock for the 8086 microprocessor are derived from a 24 MHz oscillator (location Y1). Locations 10A, 10C, 10D, 10E, 11C, 11D, 11E and 11F are used to divide to an 8 MHz clock to the CRT and a 4 MHz clock to the 8086 clock pin. Locations 10A, 10D, 11D, 12D and 12E divide the 24 MHz clock into timing signals used to generate Row Address Strobe (RAS) at locations 10B and 8B. Additionally, Column Address Strobe (CAS0 and CAS1) are also generated at locations 8A, 9A and 12C. Write Enable signals for high-byte and low-byte of both RAM segments are generated at locations 7A, 8A, 8B, 10A and 10C. Row Select, Column Select and Latch Enable for both the MPU and CRT are generated at locations 9A and 9B.

The CRT port of the memory requests a word from memory ever 2 us (500 KHz). CRT page select addresses are generated at locations 7C, 7D, 8C and 8D (page 4 of the schematics) by the 500 KHz clock rate from location 7B. If the 8086 requests a memory cycle during the CRT cycle, the memory controller uses the READY line on the 8086 microprocessor to generate wait states until the CRT cycle is finished and the memory can complete the requested 8086 memory cycle. The CRT Read cycle of one word every 2 us also provides sequential operation required for the RAM refreshing.

I/O Decoding

Reference page 4 of the schematics

The MPU Board addresses other boards in the system as I/O. PROM at location 10F is used to decode addresses A11 to A19. When I/O is addressed, M/IO goes LOW, causing the PROM's outputs to be HIGH. The conditions in which S.A EN is normally HIGH and DEN (Data Enable) becomes active and causes the EN OFFBOARD DATA signal at location 9C to go LOW, placing data on the bus. Read commands for RAM, ROM and S.A are generated by RD, RAM ADRS, ROM ADRS and S.A at locations 9D and 9E. Control signals RD, WR, DEN, DT/R and M/IO are also buffered out to other boards via buffers at location 9F.

DATA DISPLAY BOARD
(0114-2011)

Overview

Figure 4-7 is an illustrative block diagram of the Data Display board. This board provides high-voltage, deflection signals and video processing for the CRT display of the K105-D.

CRT Driver Components

Reference pages 1 and 2 of the schematics

The CRT driver components may be grouped into four functional blocks as follows:

1. Video drive - Q3, R28, CR6, CR38, R32, R31, CR3 and C35
2. Horizontal output - Q4, T1, Q5 and T2
3. Horizontal deflection - C52, L2, L1, CR5 and C53
4. Vertical deflection - U11B

Operation

Transistor Q3 operates as the video amplifier and applies the video signal to the cathode of the CRT. R28 is the load resistor connecting Q3 to the 30 VDC supply. The 30 VDC supply is composed of CR6 and C38, and the -40 VDC grid bias supply for the CRT consists of CR3 and C35. CR4 and C37 comprise the 200 VDC focus electrode supply.

The source voltage for these supplies is the high-voltage transformer, T2. Note also that T2 supplies the 10 KV for the second-anode of the CRT. The rectifier for the high-voltage is an integral part of the second-anode lead, and the filter capacitor for the high-voltage is the 600pF capacitance of the CRT aquedag coatings.

Transformer T1 and transistors Q4 and Q5 drive transformer T2. When Q5 is conducting, energy is stored in the primary of T2. When Q5 is switched off, the energy stored in the T2 primary is transferred to the secondary.

When Q5 switches off, the voltage at its collector rises to approximately 120 VDC and is impressed upon the horizontal deflection coil via L1 and L2. This voltage causes a current to flow in the deflection coil which in turn causes the electron to deflect to the left side of the CRT. The positive current flow decays in a linear manner, being zero at center screen. Because of the resonant circuit, C53 and the deflection coil, the current increases in the negative direction for the right side of the screen. At center screen Q5 again switches on and remains on until the beam is deflected to the right side of the screen. At this time, Q5 again switches off, and the process begins again.

Vertical deflection is accomplished using a TDA1270 integrated circuit, U11B. This IC contains an oscillator, a preamp and a power amp. The oscillator fre-

quency is controlled by R21, R22 and C49. The waveform is shaped by R20, R37, R42, R44, R47, C45 and C46. The waveform is amplified by the preamp and power amplifier and impressed upon the vertical deflection coil via C51. The current is sensed across R45 and returned to the preamp via feedback resistor R46.

Sync Generation

Reference page 3 of the schematics

ICs 7A, 8A, 9A and 10A are counters which are configured to provide addresses to the vertical processor PROM (8B) and the horizontal processor PROM (10B). These PROMs generate the vertical sync and horizontal drive signals.

Keyboard Processing

Reference page 4 of the schematics

ICs 13E and 14E provide keyboard interface and scanning, respectively. IC 2E is an interrupt controller which also works in conjunction with the keyboard interface.

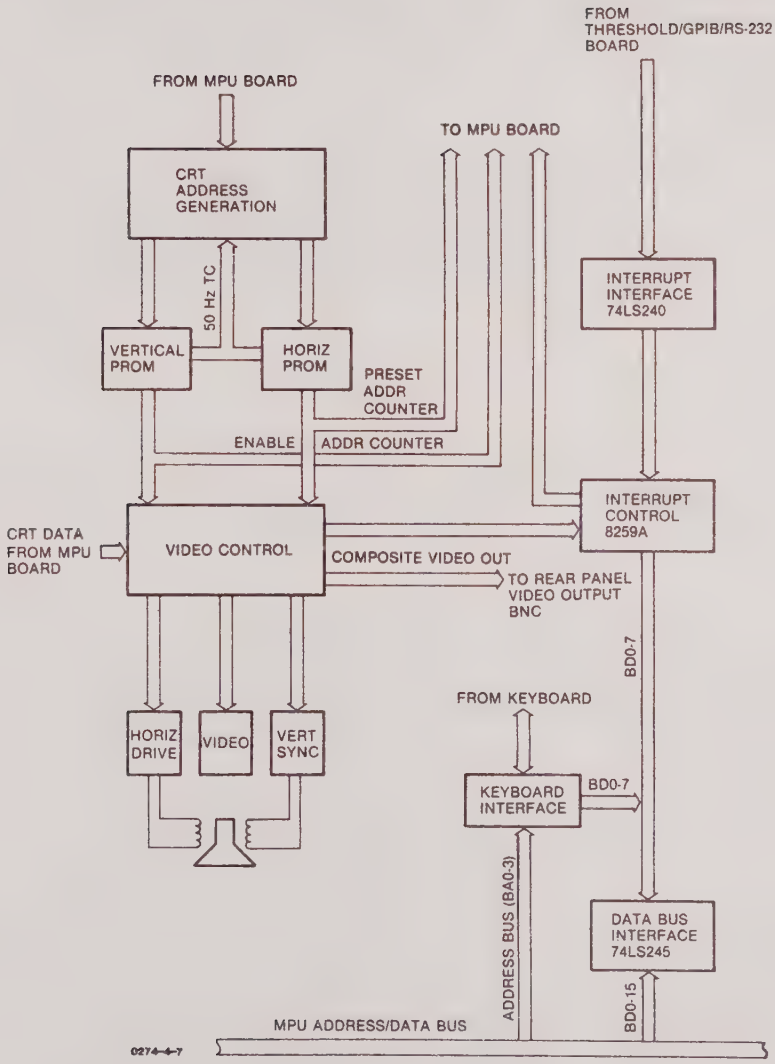


Figure 4-7. Data Display Board Block Diagram

Chapter 5

DISK DIAGNOSTICS

INTRODUCTION

This chapter provides the technician with descriptions of and instructions for the use of the diagnostic routines contained on the diagnostic disk. Routines are are present for all K105-D boards.

The K105 Diagnostic Operating System is the "user interface" or "front end" for the K105 Diagnostics. The main functions that it performs are as follows:

1. DIAG provides a menu for the operator to enter options and parameters.

The Diagnostic Operating System, or DIAG for short, allows the operator to run the Diagnostics with certain options. The individual Diagnostic modules use these options to determine program flow and operation.

These options include which boards in the system are to be tested, the number of times to repeat each test, halt Diagnostic execution upon error, loop Diagnostic execution upon error, test floppy disk drive A or B, test floppy drive side 0 or side 1, display error messages or suppress messages, and allow operator interaction of the Diagnostics.

These options and parameters are explained in a later section.

2. DIAG loads Diagnostic modules from disk and executes them.

The Diagnostic modules consist of six programs on the K105-D disk that are loaded in one at a time and executed. Due to the size of the modules (up to 40k in length) and the limited RAM space available (64k), it would be impossible for all of the code required to test the K105, to be resident in memory at once. When DIAG is testing a particular board, the appropriate Diagnostic module is then loaded in from the disk and executed.

These Diagnostic modules are discussed in a later section.

3. DIAG provides Pass/Fail History information.

DIAG keeps a tabulation of each time a test is executed, and whether it passed or failed. This information is cumulative. If the Diagnostic is run for a long period of time, the Pass/Error information is a total representation of all passes and errors.

NOTE: The maximum number of Passes or Errors DIAG can log is 65,535. If the error count reaches this limit, it does not wrap around to 0, but DIAG stops incrementing this count.

STARTING UP THE K105 DIAGNOSTICS

When The K105 Logic Analyzer is powered-up, it performs its power-on self-test diagnostics. Assuming these have passed, the Logic Analyzers's default menu is displayed.

To boot up the Disk Operating System, insert the mini floppy diskette into disk drive A with the write protect tab nearest to the activity light. Close the door on the drive.

DEpress first the "I/O" key, then "1". The display should change to the directory contents of the diskette. The following files should be in the display:

DIAG -00.EXE	(Diagnostic Operating System)
IODIAG-00.EXE	(I/O Options Diagnostic Module)
TRDIAG-00.EXE	(Trace Control Diagnostic Module)
DMDIAG-00.EXE	(Data Memory Diagnostic Module)
KDDIAG-00.EXE	(Keyboard/Display Diagnostic Module)
HSDIAG-00.EXE	(High Speed Timing Diagnostic Module)
CTDIAG-00.EXE	(Clock/Threshold Diagnostic Module)

Other files may be listed, but they are irrelevant to the Diagnostics.

IODIAG, TRDIAG, DMDIAG, KDDIAG, HSDIAG and CTDIAG are all Diagnostic modules and are not executable as stand alone programs. They are all loaded in and executed by DIAG-00.EXE. If a "RECALL" is done on one of these modules, the K105 locks up.

To load DIAG, press the NEXT key until the DOS "RECALL" selection appears. Press the right arrow key to enter the filename field. Press the down arrow key until DIAG-00.EXE is highlighted. Press the F4 key. This loads DIAG from disk and executes it. The K105 Diagnostic Main Menu is then be displayed.

DIAG MENUS AND DISPLAYS

MAIN MENU

The "Main" Menu is displayed upon booting up DIAG. This Main Menu has three main fields.

The top of the screen has a list of the keys, and a description of the function for each key. Throughout the Diagnostic execution, the top of the screen has a list of keys. The keys listed and the functions of these keys vary, depending on the particular state or menu the Diagnostic is in.

The lower-right side of the screen has a list of the "ACTIVE" boards in the system. When DIAG began to run, it peeked out to see which boards were in the K105 chasis motherboard. The boards that it found were marked as "ACTIVE", and these are the ones that it tests.

The lower-left side of the screen has a list of the "INACTIVE" boards, or the boards that are not present in the system. Some boards are optional, and since DIAG was written to test all possible components of a K105 system, boards that are not present are displayed as "INACTIVE", indicating these boards will not be tested.

NOTE: The "ACTIVE" and "INACTIVE" status can be forced or overridden. If, for example, a board is actually present in the system, but you do not wish DIAG to test it, using the up or down arrow keys you can force it INACTIVE by positioning the cursor next to the name of the board and pressing the left arrow key. This switches the board designation to the INACTIVE side. This can be done for any or all boards.

Boards that are flaged as "INACTIVE" can be forced to be "ACTIVE" by using the up and down arrow keys and positioning the cursor next to the name of the board and pressing the right arror key. This would be useful if a board is actually in the system but is faulty, and caused it to appear in the "INACTIVE" status when DIAG started up. The board can be forced "ACTIVE" and tested.

Of course if a board is not in the system, and it is forced to be "ACTIVE" and the Diagnostic is run, it will fail and give you non-relavent information.

SYSTEM TESTING, (ALL ACTIVE BOARDS).

When DIAG is started and the Main Menu is displayed, the ACTIVE/INACTIVE/-TEST>>> cursor points to "ALL ACTIVE BOARDS". If the NEXT key is pressed, all of the tests for all of the boards in the "ACTIVE" list are automatically tested sequencially.

Before each test is executed it is loaded in by DIAG and the message "LOADING DIAGNOSTIC FILE" will be displayed. The name of the current Diagnostic module is displayed at the top and the test names and test steps are updated.

During this automatic testing, DIAG displays the number of Passes and Errors at the bottom of the screen. If there are any errors, an error message is displayed at the center of the screen, and the Error count at the bottom of the screen is incremented. The Pass counter at the bottom of the screen is not be incremented until all tests for all active boards are performed.

If at any time you wish to abort the Diagnostic execution, pressing the STOP key aborts the current test and returns to the Main Menu.

System Testing is normally performed if an overall picture of the unit's integrity is desired. Since all Subtests for all ACTIVE boards is performed, this testing takes quite a while.

SINGLE BOARD TESTING.

If a single board is to be tested, the TEST>>> cursor should be positioned next to the name of the board and the next key pressed. This method is different in several ways from testing "ALL ACTIVE BOARDS".

First the testing is performed only on the chosen board. Second, the testing is not started automatically. The Subtest Menu for thintermittantly failing, the continuous looping allows the operator to trigger on a write pulse, a read pulse or a clock.

The looping continues until the LOOP ON ERROR options is disabled by pressing the EDIT key and changing the selection to "NO".
f a single board or boards is
unknown, and a direct test on the board in question is performed. This method provides information at a quicker rate than if all the previous boards in the ACTIVE list are tested.

If at any time you wish to abort the Diagnostic execution, pressing the STOP key aborts the current Subtest and return to the Subtest Menu.

ALL SUBTESTS OR INDIVIDUAL SUBTESTS

When a single board is selected for testing, the Subtest Menu is displayed. A single Subtest can be performed by positioning the highlighting cursor over the desired test and pressing the NEXT key. The single Subtest runs, and then return to the Subtest Menu. If the parameter selection for NUMBER TO REPEAT TESTS is greater than 1, the particular Subtest is repeated that number of times.

"ALL SUBTESTS" executes all of the tests in the Menu sequentially, and returns to the Subtest Menu when complete.

If at any time you wish to abort the Diagnostic execution, pressing the STOP key aborts the current Subtest and returns to the Subtest Menu.

Pressing the PREVIOUS key returns you to the Main Menu.

DIAGNOSTIC PARAMETERS (EDIT KEY)

There are a number of options or parameters for the execution of the Diagnostic modules. These parameters control the program flow of execution. The parameters can be displayed and/or changed at any time by pressing the EDIT key. This displays the list of parameters, and the current selections. Once the parameter options are selected, pressing the PREVIOUS key returns you to the previous Menu Display.

The parameters are changed by positioning the cursor next to the desired parameter and pressing the NEXT key. This selects the opposite of the currently displayed option, i.e. YES changes to NO. This method is valid for all parameters except the TIMES TO REPEAT TEST which is explained later.

The parameters are as follows:

Parameter	Options	
1. HALT ON ERROR	NO, YES	(default is NO)
2. LOOP ON ERROR	NO, YES	(default is NO)
3. DISPLAY ERROR MESSAGES	YES, NO	(default is YES)
4. TIMES TO REPEAT TEST(S)	1 - 65535	(default is 1)
5. TEST DRIVE A	NO, YES	(default is NO)
6. TEST DRIVE B	YES, NO	(default is YES)
7. TEST SIDE 0	YES, NO	(default is YES)
8. TEST SIDE 1	YES, NO	(default is YES)
9. RUN OPERATOR ACTION TESTS	NO, YES	(default is NO)

HALT ON ERROR

The first parameter, HALT ON ERROR, specifies that if during the execution of the Diagnostic an error occurs, the Diagnostic temporalily halts and the error message remains on the screen. A "HALTED ON ERROR" message blinks to verify that the Diagnostic is halted. Diagnostic execution can be resumed by pressing the NEXT key. If another error occurs, DIAG again halts until the NEXT key is pressed.

Normally when there is an error, and the HALT ON ERROR parameter is not selected, the error message is displayed on the screen for about a second. This doesn't allow adequate time to read all of the information displayed, so HALT ON ERROR is useful for "single stepping" through the errors that occur.

The disadvantage of HALT ON ERROR is that when an error occurs, all testing is suspended, and the NEXT key must be entered to resume. In the case where you want a unit to run the diagnostics for a period of time without the need of operator actions, and later you will check the number of Passes and Errors, HALT ON ERROR should be disabled by setting the option to "NO".

LOOP ON ERROR

LOOP ON ERROR specifies that if during the execution of the Diagnostic an error occurs, the Diagnostic should loop on the test step that found an error. This test step is repeated continuously even if it occasionally passes.

The LOOP ON ERROR option is useful for debugging a board. If for example a board is dule also actually calls the

Print Error Message routine in the Diagnostic Operating System, but since the option is disabled, the message is not printed.

TIMES TO REPEAT TEST(S)

This parameter controls the number of times a test is performed. Th
NOTE: The LOOP ON ERROR option has one characteristic than could be confusing. If for example the option is enabled and an error occurs, the error message is displayed as usual, and the test is repeated. The error message is only displayed for about a second, and if the test starts passing, the Diagnostic may appear to hang since no messages are being displayed and the Test Step number remains constant. The Diagnostic is not hung up, it is in fact repeating the same Test Step without error. Pressing the EDIT key to disable the LOOP ON ERROR option and pressing the PREVIOUS key allows Diagnostic execution to proceed.

DISPLAY ERROR MESSAGES

This parameter controls whether or not the error messages is displayed when errors occur.

Normally when an error occurs, and this option is set to YES, a message describing the error is displayed for about a second, then the message is cleared. For most tests, this is desired.

If a test is running that is rather lengthy, such as a RAM addressing test, and there are many errors, the screen displays many error messages. Each time a messages is displayed the Diagnostic is paused, and this actually increases the Total Test Time. If the DISPLAY ERROR MESSAGES is set to NO, this decreases the Total Test Time.

If the unit is to be run unattended, (i.e. it is not necessary to view every error message), and the maximum number of test cycles desired, this parameter should be set to NO. The total number of errors can be displayed at a later time by pressing the DATA key.

NOTE: When the DISPLAY ERROR MESSAGES is set to NO, the Diagnostic module that is currently executing still calls the Error tabulation routine and every error is counted and tabulated. The Diagnostic module also actually calls the Print Error Message routine in the Diagnostic Operating System, but since the option is disabled, the message is not printed.

TIMES TO REPEAT TEST(S)

This parameter controls the number of times a test is performed. The default is 1. This means when the test or tests are started by pressing the NEXT key, it/they are executed one time and the Diagnostic then pauses.

If several test repeats or continuous testing is desired, any number from 1 to 65,535 can be selected. Enter this parameter by positioning the cursor and pressing the NEXT key. The number to be entered is a five digit number with leading zeros.

For example if the count desired is 158, then 00158 must be entered. If a number larger than 65,535 is entered, the program complains and asks you to re-enter the number.

NOTE: If the repeat count is more than one, the DIAG cycles through all subtests of all ACTIVE boards and repeats the cycle until the repeat count has been reached.

At any time during this execution, the DATA key may be pressed to view the Pass/Error history. Pressing the PREVIOUS key resumes execution. The EDIT key may also be pressed to change any of the parameters. Pressing the PREVIOUS key then resumes execution.

TEST DRIVE A, TEST DRIVE B

This parameter refers to the floppy disk drive tests for disk drives A and B. If a drive is selected, a disk write/read test is performed on that drive, and a "scratch" disk must be used since all data on that disk is destroyed.

The default selections are A = NO, B = YES. The Diagnostic disk is residing in Disk Drive A, and a "scratch" disk should be residing in Disk Drive B. With the default selections, no operator actions are required. Drive B is tested, and Drive A is not.

If both Disk Drives are to be tested, the parameter options must be changed to A = YES, and B = YES. Each time DIAG is ready to test Disk Drive A, the Diagnostic disk has to be removed, and a scratch disk placed in the Drive. When the test is complete, the sratch disk has to be removed from Drive A, and the Diagnostic disk inserted.

This procedure requires actions to be performed by the operator, and RUN OPERATOR ACTIONS parameter must be enabled. This is explained later.

NOTE: A "scratch" disk is defined as a new or fairly new floppy diskette, that has been "formatted" using the K105 Disk Operating System Format command. The Write Protect slot must not be covered. The disk used should not contain any important data or programs since the process of Formatting and the disk drive testing distroys all data on the diskette.

TEST SIDE 0, TEST SIDE 1

This parameter also refers to the floppy disk drives testing. Each disk drive has two sides, side 0 and side 1. Normally parameters 7 and 8 are YES, and both sides are tested during the floppy disk testing.

If for example disk drive B is having errors on side 1, and no errors on side 0, setting the TEST SIDE 0 option to NO allows for more frequent testing of side 1 of the disk drive, and gives more pass/fail information at a quicker rate.

RUN OPERATOR ACTION TESTS

Some of the tests in the Diagnostic modules require the operator to perform certain actions. One example is the testing of disk drive A which requires the operator to remove the Diagnostic disk and insert a "scratch" disk, allow the test to run, then re-insert the Diagnostic disk.
Others might be the installation of RS-232 wrap-back connectors, the testing of the Keys on the K105 Keyboard, GPIB Testing, etc.

If a unit is to run the Diagnostics unattended, this parameter should be set to NO, and the specific tests that require operation actions are not

performed.

PASS/ERROR TABLUATION (DATA KEY)

At anytime during the Diagnostic Execution, the number of passes and errors can be displayed by pressing the DATA key. Pressing the PREVIOUS key returns to the previous Menu or executions. A list of the boards in the system are displayed, as well as the total number of errors as follows:

```
NUMBER OF ERRORS
TOTALS

KEYB./DISPLAY          0
CLOCK/THRESH           0
DATA MEMORY 1          0
DATA MEMORY 2          0
TRACE CONTROL          0
H.S. TIMING 1          0
H.S. TIMING 2          0
I/O OPTION             0
```

There are two fields highlighted by the cursor. They are ERRORS and TOTALS. If the cursor is over ERRORS, pressing the NEXT key changes the display to the number of Passes, (changing ERRORS to PASSES). Pressing the NEXT key again changes back to the Error display.

This ERRORS/PASSES display shows the total accumulative errors and passes for each board in the K105 System. If a board is not in the system, or it was forced INACTIVE, the Pass and Error count is 0 for that board. Otherwise, the number of times DIAG tested the board is displayed for the Passes, and the total number (if any) of errors are displayed.

If the down arrow key is pressed, this moves the cursor into the TOTALS field, and pressing the NEXT key displays the total errors/passes for each Subtest of the Keyboard/Display Board. Pressing the NEXT key again displays the total errors/passes for each Subtest of the Clock/Threshold Board.

Consecutive depressoins of the NEXT key displays the Data Memory #1, Data Memory #2, Trace Control, H.S. Timing #1, H.S. Timing #2, the I/O Option Board, and then finally back to the Main Error/Pass Display Menu.

If for example you wish to view to information about the Clock Threshold Board, perform the following steps:

Press the DATA key to display the Board list and total Error count. Press the NEXT key to display the Board list and total Pass count. Press the down arrow key and press the NEXT key twice to display the Clock/Threshold Board Subtest Pass count. Press the up arrow and then the NEXT key to display the Clock/-Threshold Board Subtest Error count.

Press the PREVIOUS key to return to the previous Menu.

SUMMARY OF K105 DIAGNOSTIC OPERATING SYSTEM KEYS

The K105 Diagnostic recognizes the following keys:

Key	Menu	Function
NEXT	Main Menu	Execute Diagnostic.
	Subtest Menu	Execute Diagnostic.
	HALTED ON ERROR	Resume Diagnostic execution.
	Parameter Menu	Change selected option.
	Pass/Error Display	Change Error display to Pass display, Cycle through Subtest lists.
PREV	Main Menu	Re-initialize Diagnostic.
	Subtest Menu	Return to Main Menu.
	Parameter Menu	Return to previous Menu or execution.
	Pass/Error Display	Return to previous Menu or execution.
EDIT	Any Menu	Display the Parameter options.
DATA	Any Menu	Display the Pass/Error information.
STOP	Any execution	Abort current test.
	HALTED ON ERROR	Abort current test.
FIELD	Main Menu	ACTIVATE/INACTIVE a Board, or Select a Board for testing.
	Subtest Menu	Select a Single or all tests.
	Parameter Menu	Select a parameter.
	Pass/Error Display	Change fields for Errors/Passes, or cycle through all Subtest lists.

K105-D DATA MEMORY BOARDS

OVERVIEW

This section describes the subtests executed on the K105-D DATA MEMORY boards, and the associated error reporting and methodology of programming.

The data memory diagnostic is divided into four subtests, each of which is described individually on the following pages.

Subtests 1 through 3 are all TTL logic related, and subtest 4 uses ECL input logic which is translated into TTL logic before being gated to the front end gate arrays.

External control signals like PC0 through PC2, 'RECORD', 'ARMD', 'LINKED', 'M-> A' are all from the trace control board. These signals were not tested in the trace control diagnostic, but will be included in the data memory diagnostics.

Gate arrays have two data output paths. In this diagnostic, we check the path PD00 through PD31; only the path TD00 through TD31 is tested in the trace control diagnostics.

If the trace control board is not installed, the data memory diagnostic will be aborted and the following information message will be displayed.

```
>TRACE CONTROL BOARD IS NOT INSTALLED
>TEST ABORTED!
```

NOTE: The 'TARGET LOGIC' listed in each subtest description does not necessarily include all of the logic which could affect the operation of that subtest.

SUBTEST CATEGORIES

1. ADDRESS MODULO COUNTER TEST
2. CPU AND RAM DATA INTEGRITY TEST
3. RAM ADDRESS INTEGRITY TEST
4. INPUT TRANSLATOR TEST

ERROR COUNT CATEGORIES

1. SUBTEST 1 ERROR COUNT
2. SUBTEST 2 ERROR COUNT
3. SUBTEST 3 ERROR COUNT
4. SUBTEST 4 PROBE A ERROR COUNT COUNT
5. SUBTEST 4 PROBE B ERROR COUNT COUNT
6. SUBTEST 4 PROBE C ERROR COUNT COUNT
7. SUBTEST 4 PROBE D ERROR COUNT COUNT

TITLE: ADDRESS MODULO COUNTER TEST

TARGET LOGIC: 19B, 18B, 17A, 13A, 9A, 5A, 18C

DESCRIPTION: The address modulo counter is functionally tested by resetting the address counter to 0 then issuing CNT clock pulses until the MSB bit is equal to 1. The number of CNT clocks issued is then verified to equal to 512.

A CNT clock pulse is issued by reading port C4H (data memory board 1) or port D4H (data memory board 2).

The MSB bit is verified by reading port C4H (data memory board 1) or port D4H (data memory board 2).

The following table indicates the operation being tested for the various diagnostic steps.

TEST STEP	OPERATION PERFORMED
1	BOARD ACTIVE CHECK
2	COUNTER MSB BIT CHECK

ERROR MESSAGE:

1. If the data memory board is not installed, the following message is displayed:

```
*TEST        FAILED--TEST        STEP        zz
TESTED DATA MEMORY BOARD NOT ACTIVE
```

where zz should be 01

2. If an address counter error occurs, the following message is displayed:

```
*TEST        FAILED--TEST        STEP        zz
TOTAL             MODULO            COUNT=ccccH
COUNT                              EXPECTED=eeeeH
```

where zz should be 02
cccc should be 0000--0200
eeee should be 0200

TITLE: CPU AND RAM DATA INTEGRITY TEST

TARGET LOGIC:

2B, 6B, 3B, 7B, 10B, 14B, 11B,
15B, 17B, 1D, 5D, 9D, 13D, 2C,
10C, 14C, 17C, 3C, 7C, 11C, 15C,
18C, 17D, 18D, 19C, 19A
and the target logic listed in subtest 1

DESCRIPTION: The CPU and RAM data logic is functionally tested by resetting the address counter to 0, issuing CNT clock pulses to increment the RAM address, writing the nibble data to each RAM location and then verifying the data by reading the same RAM location.

A CNT clock pulse is issued by reading port C4H (data memory board 1) or port D4H (data memory board 2).

All 1024 RAM locations are verified.

All acquisition RAMs are verified through all nibble patterns.

The following table indicates the RAM and the nibble data being tested for the various diagnostic test step:

TEST STEP	RAM NUMBER	NIBBLE PATTERN
03	1	0AH
04	2	0AH
05	3	0AH
06	4	0AH
07	5	0AH
08	6	0AH
09	7	0AH
10	8	0AH
11	9	0AH
12	1	05H
13	2	05H
14	3	05H
15	4	05H
16	5	05H
17	6	05H
18	7	05H
19	8	05H
20	9	05H
21	1	0CH
22	2	0CH
23	3	0CH
24	4	0CH
25	5	0CH
26	6	0CH

TEST STEP	RAM NUMBER	NIBBLE PATTERN

27	7	0CH
28	8	0CH
29	9	0CH
30	1	03H
31	2	03H
32	3	03H
33	4	03H
34	5	03H
35	6	03H
36	7	03H
37	8	03H
38	9	03H
39	1	01H
40	2	01H
41	3	01H
42	4	01H
43	5	01H
44	6	01H
45	7	01H
46	8	01H
47	9	01H
48	1	02H
49	2	02H
50	3	02H
51	4	02H
52	5	02H
53	6	02H
54	7	02H
55	8	02H
56	9	02H
57	1	04H
58	2	04H
59	3	04H
60	4	04H
61	5	04H
62	6	04H
63	7	04H
64	8	04H
65	9	04H
66	1	08H
67	2	08H
68	3	08H
69	4	08H
70	5	08H
71	6	08H
72	7	08H
73	8	08H
74	9	08H

ERROR MESSAGE:
If an error occurs,the following message is displayed:

```
*TEST FAILED--TEST STEP ss
CPU & RAM INTEGRITY TEST
TESTING RAM LOCATED AT #r
MODULO ADDRESS COUNTER=aaaaH
NIBBLE READ=nnH
NIBBLE EXPECTED=eeH

where ss should be 03--74
      #r should be 1 through 9
      aaaa should be 0000--03FF
      nn should be 00--FF
      ee should be 0A,05,0C,03,01,02,04,08
```

Data Memory Board Subtest 3

TITLE: ACQUISITION RAM ADDRESS INTEGRITY TEST

TARGET LOGIC:

2B, 6B, 3B, 7B, 10B, 14B, 11B, 15B, 17B,
1D, 5D, 9D, 13D
2C, 6C, 10C, 14C, 17C, 3C, 7C, 11C, 15C, 18C
17D, 18D, 19C, 19A
and the target logic listed in subtest 1

DESCRIPTION: The acquisition RAM address logic is functionally tested by resetting the address counter to 0, clearing all 1024 locations and then writing the nibble data 0AH to the asserted RAM location. The data is then verified by reading all 1024 RAM locations.

All RAMs will be verified through all asserted address bits.

The following table indicates the RAM and the asserted address being tested for the various diagnostic steps:

TEST STEP	ASSERTED ADDRESS LINE	NIBBLE PATTERN
75	01H	0AH
76	02H	0AH
77	04H	0AH
78	08H	0AH
79	10H	0AH
80	20H	0AH
81	40H	0AH
82	80H	0AH
83	100H	0AH
84	200H	0AH

ERROR MESSAGE: If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
RAM ADDRESS INTEGRITY TEST
TESTING RAM LOCATED AT #r
NIBBLE WRITTEN TO ADDRESS=aaaaH
NIBBLE FOUND AT ADDRESS=ffffH

where ss should be 75--84
      #r should be 1 through 9
      aaaa should be 0001,0002,0004,0008
                     0010,0020,0040,0080
                     0100,0200
      ffff should be 0000--03FF
```

Data Memory Board Subtest 4

TITLE: INPUT TRANSLATOR TEST

TARGET LOGIC: 2A, 3A, 6A, 7A, 10A, 11A, 14A, 15A
4C, 1C, 5C, 8C, 12C, 9C, 13C, 16C
2B, 6B, 3B, 7B, 10B, 14B, 11B, 15B, 17B
1D, 5D, 9D, 13D
2C, 6C, 10C, 14C, 18C
3C, 7C, 11C, 15C, 18C
17D, 18D, 19C, 19A
and the target logic listed in subtest 1

DESCRIPTION: Before testing, be sure to plug in the corresponding main channels' probes into the front end pods.

The input translator logic is functionally tested by using the 5 MHz master clock to record the data of the front end probes.

After a software time delay, the trace operation is stopped and all 1024 locations in the acquisition RAM are verified.

All pods (A, B, C, D) are verified with VAR threshold +10.0V and -9.60V.

If data memory board 1 is selected, then

POD A refers to 'A' CLK PROBE
POD B refers to 'B' CLK PROBE
POD C refers to 'C' CLK PROBE
POD D refers to 'D' CLK PROBE

If data memory board 2 is selected, then

POD A refers to 'A' F--8 PROBE
POD B refers to 'B' F--8 PROBE
POD C refers to 'C' F--8 PROBE
POD D refers to 'D' F--8 PROBE

The following table indicates the pod, probe data being tested for the various diagnostic test steps:

TEST STEP	PROBE POD	PROBE DATA
85	A CLK/A F--8	0FFH
86	A CLK/A F--8	000H
87	B CLK/B F--8	0FFH
88	B CLK/B F--8	000H
89	C CLK/C F--8	0FFH
90	C CLK/C F--8	000H
91	D CLK/D F--8	0FFH
92	D CLK/D F--8	000H

ERROR MESSAGE: If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
PROBE CHANNELS TESTED WAS p
MODULO ADDRESS COUNTER=aaaaH
PROBE DATA READ=nnH
PROBE DATA EXPECTED=eeH

where ss should be 85--92
      p should be A,B,C,D
      aaaa should be 0000--03FF
      nn should be 00--FF
      ee should be 00 OR FF
```

K105-D TRACE CONTROL BOARD

OVERVIEW

This section describes the subtests executed on the K105 TRACE CONTROL board, the associated error reporting, and the methodology of programming.

The trace control diagnostic is divided into 10 subtests, each described individually on the following pages.

Subtests 1 through 4 are basic tests; subtests 3 through 4 have two options (32 inputs and 64 inputs low speed configuration); and subtests 5 through 10 are tests of the recognition RAMs, which require only a 32 channel low speed configuration.

The trace control board output signals, such as PC0 through PC2, 'RECORD' and 'LINKED', are not tested in the trace control board diagnostics, so chips 22E and 21E are not tested now, but they will be tested as part of the data memory board diagnostics.

If the data memory board 1 or the clock threshold board is not installed when the trace control board is being tested, then the test will be aborted and the following message will be displayed:

```
>DATA MEMORY BOARD #1 IS NOT INSTALLED
>TEST ABORTED!
```

or

```
>CLOCK THRESHOLD BOARD IS NOT INSTALLED
>TEST ABORTED!
```

NOTE: The 'TARGET LOGIC' listed in each subtest description does not necessarily include all of the logic which could affect the operation of that subtest.

SUBTEST CATEGORIES

1. LEVEL LOGIC TEST
2. LOOP COUNTER TEST
3. RECOGNITION RAM TEST
4. TRACE DATA INPUTS TEST
5. DELAY COUNTER TEST
6. ADVANCE LOGIC TEST
7. ADVANCE RELATION TEST
8. TRACE RELATION TEST
9. STOP RELATION TEST
10. JUMP RELATION TEST

ERROR COUNT CATEGORIES

1. SUBTEST 1 ERROR COUNT
2. SUBTEST 2 ERROR COUNT
3. SUBTEST 3 ERROR COUNT
4. SUBTEST 4 ERROR COUNT
5. SUBTEST 5 ERROR COUNT
6. SUBTEST 6 ERROR COUNT
7. SUBTEST 7 ERROR COUNT
8. SUBTEST 8 ERROR COUNT
9. SUBTEST 9 ERROR COUNT
10. SUBTEST 10 ERROR COUNT

TITLE: LEVEL LOGIC TEST

TARGET LOGIC: 8C, 8D, 7A, 8A, 9A, 9B, 7B, 10D, 10C, 11E, 9E, 18D, 18B, 13E, 12E, 19E, 21D

DESCRIPTION: The level control logic is functionally tested by attempting to initialize the level control logic to all eight possible levels and verifying that each level was loaded correctly by reading the status port.

The following table indicates which level is being tested for the various diagnostic testernal Link Signal

5. Clock Test Error Count

   A. No CPU Clock Error Count
   B. No Internal Clock
   C. No External Clock

6. Glitch Detection Test Error Count

3	2
4	3
5	4
6	5
7	6
8	7

NOTE: The jump relation RAM (11A), advance relation RAM (11B), and jump/advance RAMs (11C, 11D) must be initialized prior to performing this test. This process is necessary in order to mask various gating logic which would otherwise interfere with the test. If the level logic test is not functional, these areas should be considered as possible causes.

ERROR MESSAGE:
If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP zz
LEVEL LOGIC TEST
LEVEL READ  xx
LEVEL EXPECTED =yy

where zz should be 01--08
      xx should be 00--07
      yy should be 00--07
```

TITLE: LOOP COUNTER TEST

TARGET LOGIC: 13D, 12B, 14D, 14C, 14B, 14A, 12C and the target logic listed in subtest 1.

DESCRIPTION: The loop counter logic is functionally tested by loading the desired level and loop count, then generating each clock by toggling between the desired level and the next level until the count reaches loop count, then verifying that the LC=0/ bit from the status port was active.

All eight possible levels should be verified through all loop count patterns.

The following table indicates the level and loop count being tested for the various diagnostic test steps.

A good data memory board 1 and a good clock threshold board must be installed in this subtest.

TEST STEP	LEVEL TESTED	LOOP COUNT PATTERN
9	4	0
10 through 17	0 through 7	0800h (msb)
18 through 25	0 through 7	0400h
26 through 33	0 through 7	0200h
34 through 41	0 through 7	0100h
42 through 49	0 through 7	0080h
50 through 57	0 through 7	0040h
58 through 65	0 through 7	0020h
66 through 73	0 through 7	0010h
74 through 81	0 through 7	0008h
82 through 89	0 through 7	0004h
90 through 97	0 through 7	0002h
98 through 105	0 through 7	0001h

NOTE: The jump relation RAM (11A), advance relation RAM (11B), and jump/advance RAMs (11C and 11D) must be initialized prior to performing this test. This process is necessary in order to mask various gating logic which would otherwise interfere with the test. If the loop counter is not functional, these areas should be considered as possible causes.

ERROR MESSAGE:
If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
LOOP COUNTER TEST
COUNTER EXPECTED=ppppH
LEVEL AT =zz
LOOP COUNT(LC=0/)

where ss should be 9--105
      pppp should be 0, 800, 400, 200
```

```
                    100, 80, 40, 20, 10
                    08, 04, 02, 01
zz should be 0--7
```

TITLE: RECOGNITION RAM TEST

TARGET LOGIC: 2C, 2D, 4C, 5C, 5D, 6D, 6C, 4D, 3D, 3C, 1E, 2E, 5E, 6E, 8E, 7E, 4E, 3E, 1B, 4B, 5B, 3B, 2B

DESCRIPTION: The recognition RAMs' data integrity is functionally tested by loading the address from the data memory board via the CPU Data Pass Through, and writing the data into the RAM through a transceiver, then verifying by reading the RAM data from the same transceiver.

The RAMs have 10 address lines. A6 through A0 are the trace data lines from data memory board 1, and they are latched in by the diagnostic clock. A9 through A7 are controlled by the level logic.

All eight possible levels should be verified through all data patterns.

Two options can be selected via the diagnostic monitor:

1. 32 inputs if data memory board 2 is not active
2. 64 inputs if data memory board 2 is active

The following information message is displayed:

>hh INPUTS SELECTED

where hh should be 32, 64

A good data memory board 1 and a good clock threshold board must be installed in this subtest.

The following table indicates the level, RAM, and nibble data pattern being tested for the various diagnostic test steps.

TEST STEP	LEVEL TESTED	RAM LOCATED	NIBBLE
106 through 113	0 through 7	2C	5
114 through 121	0 through 7	2D	5
122 through 129	0 through 7	4C	5
130 through 137	0 through 7	5C	5
138 through 145	0 through 7	5D	5
146 through 153	0 through 7	6D	5
154 through 161	0 through 7	6C	5
162 through 169	0 through 7	4D	5
170 through 177	0 through 7	3D	5
178 through 185	0 through 7	3C	5
186 through 193	0 through 7	2C	A
194 through 201	0 through 7	2D	A
202 through 209	0 through 7	4C	A
210 through 217	0 through 7	5C	A
218 through 225	0 through 7	5D	A

226 through 233	0 through 7	6D	A
234 through 241	0 through 7	6C	A
242 through 249	0 through 7	4D	A
250 through 257	0 through 7	3D	A
258 through 265	0 through 7	3C	A
266 through 273	0 through 7	2C	3
274 through 281	0 through 7	2D	3
282 through 289	0 through 7	4C	3
290 through 297	0 through 7	5C	3
298 through 305	0 through 7	5D	3
306 through 313	0 through 7	6D	3
314 through 321	0 through 7	6C	3
322 through 329	0 through 7	4D	3
330 through 337	0 through 7	3D	3
338 through 345	0 through 7	3C	3
346 through 353	0 through 7	2C	C
354 through 361	0 through 7	2D	C
362 through 369	0 through 7	4C	C
370 through 377	0 through 7	5C	C
378 through 385	0 through 7	5D	C
386 through 393	0 through 7	6D	C
394 through 401	0 through 7	6C	C
402 through 409	0 through 7	4D	C
410 through 417	0 through 7	3D	C
418 through 425	0 through 7	3C	C
426 through 433	0 through 7	2C	8
434 through 441	0 through 7	2D	8
442 through 449	0 through 7	4C	8
450 through 457	0 through 7	5C	8
458 through 465	0 through 7	5D	8
466 through 473	0 through 7	6D	8
474 through 481	0 through 7	6C	8
482 through 489	0 through 7	4D	8
490 through 497	0 through 7	3D	8
498 through 505	0 through 7	3C	8
506 through 513	0 through 7	2C	4
514 through 521	0 through 7	2D	4
522 through 529	0 through 7	4C	4
530 through 537	0 through 7	5C	4
538 through 545	0 through 7	5D	4
546 through 553	0 through 7	6D	4
554 through 541	0 through 7	6C	4
562 through 569	0 through 7	4D	4
570 through 577	0 through 7	3D	4
578 through 585	0 through 7	3C	4
586 through 513	0 through 7	2C	2
594 through 601	0 through 7	2D	2
602 through 609	0 through 7	4C	2
610 through 617	0 through 7	5C	2
618 through 625	0 through 7	5D	2
626 through 633	0 through 7	6D	2
634 through 641	0 through 7	6C	2
642 through 649	0 through 7	4D	2
650 through 657	0 through 7	3D	2

TEST STEP	LEVEL TESTED	RAM LOCATED	NIBBLE
658 through 665	0 through 7	3C	2
666 through 673	0 through 7	2C	1
674 through 681	0 through 7	2D	1
682 through 689	0 through 7	4C	1
690 through 697	0 through 7	5C	1
698 through 705	0 through 7	5D	1
706 through 713	0 through 7	6D	1
714 through 721	0 through 7	6C	1
722 through 729	0 through 7	4D	1
730 through 737	0 through 7	3D	1
738 through 745	0 through 7	3C	1

ERROR MESSAGE:
If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
RECOGNITION RAM TEST
RAM LOCATION AT= rr
LEVEL AT= zz
ADDRESS AT=aaH
NIBBLE READ=ddH
NIBBLE EXPECTED=yyH

where ss should be 106--745
      rr should be 2C, 2D, 4C, 5C, 5D, 6D, 6C, 4D, 3D, 3C
      zz should be 0--7
      aa should be 00--7F
      dd should be 00--0F
      yy should be 05, 0A, 03, 0C, 08, 04, 02, 01
```

TITLE: TRACE DATA INPUTS TEST

TARGET LOGIC : 2C, 2D, 4C, 5C, 5D, 6D, 6C, 4D, 3D, 3C, 1E, 2E, 5E, 6E, 8E, 7E, 4E, 3E, 1B, 4B, 5B, 3B, 2B

DESCRIPTION: The trace data inputs are functionally tested by loading the asserted trace data input from data memory board 1 via the 'CPU Data Pass Through' as the asserted RAM address. Nibble data 0AH is then written into the RAM via the transceiver. The data is then verified by reading the RAM data from the same transceiver port for all possible 128 locations at the selected level.

The RAMs have 10 address lines, A6 through A0 are the trace data lines from data memory board 1, latched in by the diagnostic clock. A9 through A7 are controlled by the level logic.

All eight possible levels should be verified through all 128 locations with nibble data 0AH.

Two options can be selected via the diagnostic monitor:

1. 32 inputs if data memory board 2 is not active
2. 64 inputs if data memory board 2 is active

The following information message is then displayed:

>hh INPUTS SELECTED

where hh should be 32, 64

A good data memory board 1 and a good clock threshold board must be installed in this subtest.

The following table indicates which RAM and the associated asserted trace data line is being tested for the various diagnostic test steps. This test always uses nibble data 0AH and level 4 for all test steps.

TEST STEP	RAM LOCATED	ADDRESS TESTED	TD LINE
746	2C	01H	TD04
747	2C	02H	TD05
748	2C	08H	TD03
749	2C	10H	TD02
750	2C	20H	TD01
751	2C	40H	TD00
752	2D	01H	TD08
753	2D	02H	TD06
754	2D	04H	TD07
755	2D	08H	TD09
756	2D	10H	TD10
757	2D	20H	TD11

TEST STEP	RAM LOCATED	ADDRESS TESTED	TD LINE
758	2D	40H	TD12
759	4C	01H	TD14
760	4C	02H	TD15
761	4C	08H	TD13
762	4C	10H	TD16
763	4C	20H	TD17
764	4C	40H	TD18
765	5C	01H	TD23
766	5C	02H	TD24
767	5C	04H	TD25
768	5C	08H	TD22
769	5C	10H	TD21
770	5C	20H	TD20
771	5C	40H	TD19
772	5D	01H	TD27
773	5D	02H	TD26
774	5D	08H	TD28
775	5D	10H	TD29
776	5D	20H	TD30
777	5D	40H	TD31
778	6D	01H	TD59
779	6D	02H	TD58
780	6D	08H	TD60
781	6D	10H	TD61
782	6D	20H	TD62
783	6D	40H	TD63
784	6C	01H	TD55
785	6C	02H	TD56
786	6C	04H	TD57
787	6C	08H	TD54
788	6C	10H	TD53
789	6C	20H	TD52
790	6C	40H	TD51
791	4D	01H	TD50
792	4D	02H	TD49
793	4D	04H	TD48
794	4D	10H	TD45
795	4D	20H	TD46
796	4D	40H	TD47
797	3D	01H	TD42
798	3D	02H	TD41
799	3D	04H	TD40
800	3D	08H	TD43
801	3D	10H	TD44
802	3D	20H	TD39
803	3D	40H	TD38
804	3C	01H	TD36
805	3C	02H	TD37
806	3C	08H	TD35
807	3C	10H	TD34
808	3C	20H	TD33
809	3C	40H	TD32

ERROR MESSAGE:
If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
TRACE DATA INPUTS TEST
TD xx----TD yy LINES BEEN TESTED
WROTE TO ADDRESS=aaH
FOUND AT ADDRESS=ffH
where ss should be 746--809
      xx should be 00--63
      yy should be 00--63
      aa should be 00--7F
      ff should be 00--7F
```

TITLE: DELAY COUNTER TEST

TARGET LOGIC : 15A, 15B, 15C, 15D, 16A, 16B, 16C, 16D, 17A, 17B, 17C, 17D.

DESCRIPTION: The delay counter is functionally tested by loading the delay count pattern into RAMs (15A, 15B, 15C and 15D) and enabling the 100khz master clock to 'up count' the S169 counters (17A, 17B, 17C and 17D). After the specified software time delay, the '=' output from the 4 bit comparator (16A) propagates through the advance multiplexer (10B) and advances the selected level. The 'LINKED' signal also becomes true at this time.

The advanced level and the 'LINKED' signals are verified by reading status port E0H, bit 4 for the 'LINKED' signal, bits 3 through 1 for the advanced level.

All eight possible levels should be verified through all 16 delay count patterns.

The methodology used is similar to the command:

"WAIT FOR <1..65535> CLOCKS"

A good data memory board 1 and a good clock threshold board must be installed in this subtest.

The following table indicates the delay expression, associated level, and delay count pattern being tested for the various diagnostic test steps.

TEST STEP	LEVEL TESTED	DELAY COUNT	DELAY EXPRESSION TYPE
810 through 817	0 through 7	8000H	CLOCKS
818 through 825	0 through 7	4000H	CLOCKS
826 through 833	0 through 7	2000H	CLOCKS
834 through 841	0 through 7	1000H	CLOCKS
842 through 849	0 through 7	0800H	CLOCKS
850 through 857	0 through 7	0400H	CLOCKS
858 through 865	0 through 7	0200H	CLOCKS
866 through 873	0 through 7	0100H	CLOCKS
874 through 881	0 through 7	0080H	CLOCKS
882 through 889	0 through 7	0040H	CLOCKS
890 through 897	0 through 7	0020H	CLOCKS
898 through 905	0 through 7	0010H	CLOCKS
906 through 913	0 through 7	0008H	CLOCKS
914 through 921	0 through 7	0004H	CLOCKS
922 through 929	0 through 7	0002H	CLOCKS
930 through 937	0 through 7	0001H	CLOCKS

ERROR MESSAGE:
If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
DELAY COUNTER TEST
DELAY COUNT=ccccH
DELAY EXPRESSION=CLOCKS
LEVEL READ=rr
LEVEL EXPECTED=vv
LINKED ON ADVANCE NOT TRUE

where ss should be 810--937
      cccc should be 8000, 4000, 2000, 1000
                     0800, 0400, 0200, 0100
                     0080, 0040, 0020, 0010
                     0008, 0004, 0002, 0001
      rr should be 00--07
      vv should be 00--07
```

TITLE: ADVANCE LOGIC TEST

TARGET LOGIC: 15A, 15B, 15C, 15D, 16A, 16B, 16C, 16D, 17A, 17B, 17C, 17D, 11B and related logic gates.

DESCRIPTION: The advance logic is functionally tested by loading the delay count pattern into RAMs (15A, 15B, 15C and 15D) and using the trace data inputs lines of the lower 32 inputs as the advance event address.

The event is toggled between "TRUE" and "FALSE" to 'up count' the S169 counters (17A, 17B, 17C and 17D) until the delay count has been reached. The "=" output from the 4 bit comparator (16A) propagates through the advance multiplexer (10B) and advances the selected level.

The 'LINKED' signal also becomes true at this time. Whenever the trace data inputs TD00 through TD31 equal AAAAAAAAH, the advance event is true. If TD00 through TD31 is not equal to AAAAAAAAH, the event is not true.

The advanced level and 'LINKED' signals are verified by reading status port E0H, bit 4 for the 'LINKED' signal, and bits 3 through 1 for the advanced level.

All eight possible levels should be verified through all 16 delay count patterns.

The methodology used is similar to the command:

"WAIT FOR <1..65535> OCCURRENCE OF SAMPLE=<pattern>"

A good data memory board 1 and a good clock threshold board must be installed in this subtest.

The following table indicates the delay expression, associated level, and delay count pattern being tested for the various diagnostic test steps.

TEST STEP	LEVEL TESTED	DELAY COUNT	DELAY EXPRESSION TYPE
938 through 945	0 through 7	8000H	SAMPLE=<pattern>
946 through 953	0 through 7	4000H	SAMPLE=<pattern>
954 through 961	0 through 7	2000H	SAMPLE=<pattern>
962 through 969	0 through 7	1000H	SAMPLE=<pattern>
970 through 977	0 through 7	0800H	SAMPLE=<pattern>
978 through 985	0 through 7	0400H	SAMPLE=<pattern>
986 through 993	0 through 7	0200H	SAMPLE=<pattern>
994 through 1001	0 through 7	0100H	SAMPLE=<pattern>
1002 through 1009	0 through 7	0080H	SAMPLE=<pattern>
1010 through 1017	0 through 7	0040H	SAMPLE=<pattern>
1018 through 1025	0 through 7	0020H	SAMPLE=<pattern>
1026 through 1033	0 through 7	0010H	SAMPLE=<pattern>
1034 through 1041	0 through 7	0008H	SAMPLE=<pattern>

TEST STEP	LEVEL TESTED	DELAY COUNT	DELAY EXPRESSION TYPE
1042 through 1049	0 through 7	0004H	SAMPLE=<pattern>
1050 through 1057	0 through 7	0002H	SAMPLE=<pattern>
1058 through 1065	0 through 7	0001H	SAMPLE=<pattern>

ERROR MESSAGE:
If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
ADVANCE LOGIC TEST
DELAY COUNT=ccccH
DELAY EXPRESSION:SAMPLE=<pattern>
LEVEL READ=rr
LEVEL EXPECTED=vv
LINKED ON ADVANCE NOT TRUE

where ss should be 938--1065
      cccc should be 8000, 4000, 2000, 1000
                     0800, 0400, 0200, 0100
                     0080, 0040, 0020, 0010
                     0008, 0004, 0002, 0001
      rr should be 00--07
      vv should be 00--07
```

TITLE: ADVANCE RELATION TEST

TARGET LOGIC: 15A, 15B, 15C, 15D, 16A, 16B, 16C, 16D, 17A, 17B, 13C, 13B, 11B, 10B, 21C and related logic gates.

DESCRIPTION: The advance relation is functionally tested by loading the selected relation data into the advance relation RAM 11B and the delay count pattern into RAMs (15A, 15B, 15C and 15D). Use the trace data inputs lines of the lower 32 inputs as the advance event address.

The event is forced true by gating the trace data inputs AAAAAAAAH from data memory board 1 into the lower 32 inputs of recognition RAMs. Then using the controlled master clock, the F251 counters 16A, 16B, 16C and 16D are °down counted'.

After the specified relation between the delay count and the F251 counters comes true, the specified relation output of the four bit comparator propagates through the advance multiplexer (10B) and advances the selected level.

The 'LINKED' signal also becomes true.

Whenever the trace data inputs TD00 through TD31 equals AAAAAAAAH, then the advance event is true. If TD00 through TD31 is not equal to AAAAAAAAH, then the event is not true.

The advanced level and the 'LINKED' signal are verified by reading status port E0H, bit 4 for the 'LINKED' signal, and bits 3 through 1 for the advanced level.

All eight possible levels should be verified through the count pattern 8000H and six relations.

The methodology used is similar to the command:

"WAIT UNTIL SAMPLE=<pattern> AND COUNT <rel> <delay>"

A good data memory board 1 and a good clock threshold board must be installed in this subtest.

The following table indicates the delay expression, associated level being tested for the various diagnostic test steps.

TEST STEP	LEVEL TESTED	CONDITION TYPE
1066 through 1073	0 through 7	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1074 through 1081	0 through 7	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1082 through 1089	0 through 7	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1090 through 1097	0 through 7	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1098 through 1105	0 through 7	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1106 through 1113	0 through 7	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1114 through 1121	0 through 7	SAMPLE=<pattern> AND COUNT < DELAY FALSE
1122 through 1129	0 through 7	SAMPLE=<pattern> AND COUNT = DELAY FALSE
1130 through 1137	0 through 7	SAMPLE=<pattern> AND COUNT > DELAY FALSE
1138 through 1145	0 through 7	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
1146 through 1153	0 through 7	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
1154 through 1161	0 through 7	SAMPLE=<pattern> AND COUNT <> DELAY FALSE

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
ADV RELATION TEST
CONDITION:SAMPLE=<pattern> AND COUNT rl DELAY
LEVEL READ=rr
LEVEL EXPECTED=vv
LINKED ON ADVANCE NOT TRUE
COUNTER EXPECTED=ccccH
RELATION COUNT READ=ddddH

where ss should be 1066--1162
      rl should be <,=,>,<=,>=,<>
      rr should be 00--07
      vv should be 00--07
      cccc should be expected count when condition TRUE
      dddd should be 0000 through FFFF
```

TITLE: TRACE RELATION TEST

TARGET LOGIC: 15A, 15B, 15C, 15D, 16A, 16B, 16C, 16D, 17A, 17B, 13C, 13B, 22A, 22B, 22C, 21C, 22D and related logic gates.

DESCRIPTION: The trace relation is functionally tested by loading the selected relation into the trace relationship RAM (20A) and the delay count pattern into RAMs (15A, 15B, 15C and 15D). Use the trace data inputs lines of the lower 32 inputs as the trace event address.

The trace event is forced true by gating trace data inputs AAAAAAAAH from data memory board 1 into the lower 32 inputs of recognition RAMs. Then using the controlled master clock, the F251 counters (16A, 16B, 16C and 16D) are 'down counted'.

After the specified relation between the delay count and the S169 counters becomes true, then the designated relationship output of the four bit comparator (16A) propagates through the trace multiplexer and the selected level doesn't change.

The 'LINKED' signal also becomes true. Whenever the trace data inputs TD00 through TD31 equal to AAAAAAAAH, the trace event is true. If TD00 through TD31 does not equal to AAAAAAAAH, the trace event is not true.

The 'LINKED' signal and the selected level are verified by reading the status port E0H, bit 4 for the 'LINKED' signal, bits 3 through 1 for the selected level.

All eight possible levels should be verified through the delay count pattern 8000H and all six relations: =, >, >=, <, <=, <>.

The methodology used is similar to the command:

"TRACE IF SAMPLE=<pattern> AND COUNT <rel> <delay>"

A good data memory board 1 and a good clock threshold board must be installed in this subtest.

The following table indicates the delay expression and associated level being tested for the various diagnostic test steps.

TEST STEP	LEVEL TESTED	CONDITION TYPE
1163 through 1171	0 through 7	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1172 through 1179	0 through 7	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1180 through 1187	0 through 7	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1188 through 1195	0 through 7	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1196 through 1203	0 through 7	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1204 through 1211	0 through 7	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1212 through 1219	0 through 7	SAMPLE=<pattern> AND COUNT < DELAY FALSE
1220 through 1227	0 through 7	SAMPLE=<pattern> AND COUNT = DELAY FALSE
1228 through 1235	0 through 7	SAMPLE=<pattern> AND COUNT > DELAY FALSE
1236 through 1243	0 through 7	SAMPLE=<pattern> AND COUNT <= DELAY FALSE

TEST STEP	LEVEL TESTED	CONDITION TYPE
1244 through 1251	0 through 7	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
1252 through 1259	0 through 7	SAMPLE=<pattern> AND COUNT <> DELAY FALSE

ERROR MESSAGE:
If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
TRC. RELATION TEST
CONDITION:SAMPLE=<pattern> AND COUNT rl DELAY
LEVEL READ=rr
LEVEL EXPECTED=vv
LINKED ON TRACE NOT TRUE
COUNTER EXPECTED=ccccH
RELATION COUNT READ=dddH

where ss should be 1163--1259
      rl should be <,=,>,<=,>=,<>
      rr should be 00--07
      vv should be 0007
      cccc should be expected count when condition becomes
      true
      dddd should be 0000 through FFFF
```

NOTE: If dddd<cccc, the tested relation is possibly stuck true.
If dddd>cccc, the tested relation is possibly stuck false.

TITLE: STOP RELATION TEST

TARGET LOGIC: 15A, 15B, 15C, 15D, 16A, 16B, 16C, 16D, 17A, 17B, 13C, 13B, 22A, 22B, 22C, 22D and related logic gates.

DESCRIPTION: The stop relation is functionally tested by loading the selected relationship into the stop relation RAM (20B) and the delay count pattern into RAMs (15A, 15B, 15C and 15D). Use the trace data inputs lines of the lower 32 inputs as the stop event address.

The stop event is forced true by gating the trace data inputs AAAAAAAAH from data memory board 1 into the lower 32 inputs recognition RAMs.

Then using the controlled master clock, the F251 counters 16A, 16B, 16C and 16D are 'down counted' until the stop relationship between the delay count and F251 counters become true, then the designated relationship output of the four bit comparator (16A) propagates through the trace multiplexer and the selected stop level will not change. The 'STPD/' signal also becomes true.

Whenever the trace data inputs TD00 through TD31 equals AAAAAAAAH then the stop event is true. If TD00 through TD31 is not equal to AAAAAAAAH then the stop event is not true. The 'STPD/' signal and the selected stop level is verified by reading the status port E0H, bit 6 for the 'STPD/' signal, bit 3 through 1 for stop level.

All eight possible levels should be verified through the delay count pattern 8000H and all six relations.

The methodology used is similar to the command:

"OR STOP IF SAMPLE=<pattern> AND COUNT <rel> <delay>"

A good data memory board 1 and a good clock threshold board must be installed in this subtest.

The following table indicates the delay expression and associated level being tested for the various diagnostic test steps.

TEST STEP	LEVEL TESTED	CONDITION TYPE
1260 through 1267	0 through 7	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1268 through 1275	0 through 7	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1276 through 1283	0 through 7	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1284 through 1291	0 through 7	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1292 through 1299	0 through 7	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1300 through 1307	0 through 7	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1308 through 1315	0 through 7	SAMPLE=<pattern> AND COUNT < DELAY FALSE
1316 through 1323	0 through 7	SAMPLE=<pattern> AND COUNT = DELAY FALSE
1324 through 1331	0 through 7	SAMPLE=<pattern> AND COUNT > DELAY FALSE
1332 through 1339	0 through 7	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
1340 through 1347	0 through 7	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
1348 through 1355	0 through 7	SAMPLE=<pattern> AND COUNT <> DELAY FALSE

ERROR MESSAGE:
If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
STOP RELATION TEST
CONDITION:SAMPLE=<pattern> AND COUNT rl DELAY
LEVEL READ=rr
LEVEL EXPECTED=vv
STOP OUTPUT(STPD/) NOT ACTIVE
COUNT EXPECTED=ccccH
RELATION COUNT READ=ddddH

where ss should be 1260--1355
      rl should be <,=,>,<=,>=,<>
      rr should be 00--07
      vv should be 00--07
      cccc should be expected count when condition becomes
      true
      dddd should be 0000 through FFFF
```

NOTE: If dddd<cccc, the tested relationship is possibly stuck true. If dddd>cccc, the tested relationship is possibly stuck false.

TITLE: JUMP RELATION TEST

TARGET LOGIC: 15A, 15B, 15C, 15D, 16A, 16B, 16C, 16D, 17A, 17B, 13C, 13B, 11A, 10A and related logic gates.

DESCRIPTION: The jump relation is functionally tested by loading the selected relation into the jump relation RAM (11A) and the delay count pattern into RAMs (15A, 15B, 15C and 15D). Use the trace data inputs lines of the lower 32 inputs as the jump event address.

The jump event is forced true by gating the trace data inputs AAAAAAAAH from the lower 32 inputs data memory board 1 into the recognition RAMs.

Then using the controlled master clock, the F251 counters 16A, 16B, 16C and 16D are 'down counted' until the designated jump relationship between the delay count and the F251 counters become true. Then the jump relation output of the four bit comparator propagates through the jump multiplexer (10A) and the previous level jump to the desired level.

The 'LINKED' signal also becomes true. Whenever the trace data inputs TD00 through TD31 equal AAAAAAAAH, the jump event is true. If TD00 through TD31 does not equal to AAAAAAAAH, the jump event is not true.

The 'LINKED' signal and the jumped level are verified by reading status port E0H, bit 4 for the 'LINKED' signal, bits 3 through 1 for the jumped level.

All eight possible levels should be verified through the delay count pattern 8000H and all six relations.

The methodology used is similar to the command:

"OR GOTO level IF SAMPLE=<pattern> AND COUNT <rel> <delay>"

A good data memory board 1 and a good clock threshold board must be installed in this subtest.

The table on the next page indicates the delay expression, and associated level being tested for the various diagnostic test steps.

TEST STEP	LEVEL TESTED	JUMP TO	CONDITION TYPE
1356 through 1363	0 through 7	0	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1364 through 1371	0 through 7	0	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1372 through 1379	0 through 7	0	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1380 through 1387	0 through 7	0	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1388 through 1395	0 through 7	0	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1396 through 1403	0 through 7	0	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1404 through 1411	0 through 7	1	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1412 through 1419	0 through 7	1	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1420 through 1427	0 through 7	1	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1428 through 1435	0 through 7	1	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1436 through 1443	0 through 7	1	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1444 through 1451	0 through 7	1	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1452 through 1459	0 through 7	2	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1460 through 1467	0 through 7	2	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1468 through 1475	0 through 7	2	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1476 through 1483	0 through 7	2	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1484 through 1491	0 through 7	2	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1492 through 1499	0 through 7	2	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1500 through 1507	0 through 7	3	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1508 through 1515	0 through 7	3	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1516 through 1523	0 through 7	3	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1524 through 1531	0 through 7	3	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1532 through 1539	0 through 7	3	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1540 through 1547	0 through 7	3	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1548 through 1555	0 through 7	4	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1556 through 1563	0 through 7	4	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1564 through 1571	0 through 7	4	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1572 through 1579	0 through 7	4	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1580 through 1587	0 through 7	4	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1588 through 1595	0 through 7	4	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1596 through 1603	0 through 7	5	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1604 through 1611	0 through 7	5	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1612 through 1619	0 through 7	5	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1620 through 1627	0 through 7	5	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1628 through 1635	0 through 7	5	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1636 through 1643	0 through 7	5	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1644 through 1651	0 through 7	6	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1652 through 1659	0 through 7	6	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1660 through 1667	0 through 7	6	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1668 through 1675	0 through 7	6	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1676 through 1683	0 through 7	6	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1684 through 1691	0 through 7	6	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1692 through 1699	0 through 7	7	SAMPLE=<pattern> AND COUNT < DELAY TRUE
1700 through 1707	0 through 7	7	SAMPLE=<pattern> AND COUNT = DELAY TRUE
1708 through 1715	0 through 7	7	SAMPLE=<pattern> AND COUNT > DELAY TRUE
1716 through 1723	0 through 7	7	SAMPLE=<pattern> AND COUNT <= DELAY TRUE
1724 through 1731	0 through 7	7	SAMPLE=<pattern> AND COUNT >= DELAY TRUE
1732 through 1739	0 through 7	7	SAMPLE=<pattern> AND COUNT <> DELAY TRUE
1740 through 1747	0 through 7	0	SAMPLE=<pattern> AND COUNT < DELAY FALSE
1748 through 1755	0 through 7	0	SAMPLE=<pattern> AND COUNT = DELAY FALSE
1756 through 1761	0 through 7	0	SAMPLE=<pattern> AND COUNT > DELAY FALSE
1762 through 1769	0 through 7	0	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
1770 through 1777	0 through 7	0	SAMPLE=<pattern> AND COUNT >= DELAY FALSE

TEST STEP	LEVEL TESTED	JUMP TO	CONDITION TYPE
1778 through 1785	0 through 7	0	SAMPLE=<pattern> AND COUNT <> DELAY FALSE
1786 through 1793	0 through 7	1	SAMPLE=<pattern> AND COUNT < DELAY FALSE
1794 through 1801	0 through 7	1	SAMPLE=<pattern> AND COUNT = DELAY FALSE
1802 through 1809	0 through 7	1	SAMPLE=<pattern> AND COUNT > DELAY FALSE
1810 through 1817	0 through 7	1	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
1818 through 1825	0 through 7	1	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
1826 through 1833	0 through 7	1	SAMPLE=<pattern> AND COUNT <> DELAY FALSE
1834 through 1841	0 through 7	2	SAMPLE=<pattern> AND COUNT < DELAY FALSE
1842 through 1849	0 through 7	2	SAMPLE=<pattern> AND COUNT = DELAY FALSE
1850 through 1857	0 through 7	2	SAMPLE=<pattern> AND COUNT > DELAY FALSE
1858 through 1865	0 through 7	2	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
1866 through 1873	0 through 7	2	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
1874 through 1881	0 through 7	2	SAMPLE=<pattern> AND COUNT <> DELAY FALSE
1882 through 1889	0 through 7	3	SAMPLE=<pattern> AND COUNT < DELAY FALSE
1890 through 1897	0 through 7	3	SAMPLE=<pattern> AND COUNT = DELAY FALSE
1898 through 1905	0 through 7	3	SAMPLE=<pattern> AND COUNT > DELAY FALSE
1906 through 1913	0 through 7	3	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
1914 through 1921	0 through 7	3	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
1922 through 1929	0 through 7	3	SAMPLE=<pattern> AND COUNT <> DELAY FALSE
1930 through 1937	0 through 7	4	SAMPLE=<pattern> AND COUNT < DELAY FALSE
1938 through 1945	0 through 7	4	SAMPLE=<pattern> AND COUNT = DELAY FALSE
1946 through 1953	0 through 7	4	SAMPLE=<pattern> AND COUNT > DELAY FALSE
1954 through 1961	0 through 7	4	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
1962 through 1969	0 through 7	4	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
1970 through 1977	0 through 7	4	SAMPLE=<pattern> AND COUNT <> DELAY FALSE
1978 through 1985	0 through 7	5	SAMPLE=<pattern> AND COUNT < DELAY FALSE
1986 through 1993	0 through 7	5	SAMPLE=<pattern> AND COUNT = DELAY FALSE
1994 through 2001	0 through 7	5	SAMPLE=<pattern> AND COUNT > DELAY FALSE
2002 through 2009	0 through 7	5	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
2010 through 2017	0 through 7	5	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
2018 through 2025	0 through 7	5	SAMPLE=<pattern> AND COUNT <> DELAY FALSE
2026 through 2033	0 through 7	6	SAMPLE=<pattern> AND COUNT < DELAY FALSE
2034 through 2041	0 through 7	6	SAMPLE=<pattern> AND COUNT = DELAY FALSE
2042 through 2049	0 through 7	6	SAMPLE=<pattern> AND COUNT > DELAY FALSE
2050 through 2057	0 through 7	6	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
2058 through 2065	0 through 7	6	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
2066 through 2073	0 through 7	6	SAMPLE=<pattern> AND COUNT <> DELAY FALSE
2074 through 2081	0 through 7	7	SAMPLE=<pattern> AND COUNT < DELAY FALSE
2082 through 2089	0 through 7	7	SAMPLE=<pattern> AND COUNT = DELAY FALSE
2090 through 2097	0 through 7	7	SAMPLE=<pattern> AND COUNT > DELAY FALSE
2098 through 2105	0 through 7	7	SAMPLE=<pattern> AND COUNT <= DELAY FALSE
2106 through 2113	0 through 7	7	SAMPLE=<pattern> AND COUNT >= DELAY FALSE
2114 through 2121	0 through 7	7	SAMPLE=<pattern> AND COUNT <> DELAY FALSE

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP ss
JUMP RELATION TEST
CONDITION:SAMPLE=<pattern> AND COUNT rl DELAY
LEVEL READ=rr
LEVEL EXPECTED=vv
LINKED ON JUMP NOT TRUE
COUNTER EXPECTED=ccccH
RELATION COUNT READ=ddddH

where ss should be 1356--2125
      rl should be <,=,>,<=,>=,<>
      rr should be 00--07
      vv should be 00--07
      cccc should be expected count when condition becomes
      true
      dddd shouls be 0000 through FFFF
```

NOTE: If dddd<cccc, the testing relation might be stuck TRUE. If dddd>cccc, thetesting relation might be stuck FALSE.

K105-D HIGH SPEED MEMORY BOARD

OVERVIEW

This section describes the subtests executed on the K105-D High Speed Memory Board (HS), the associated error reporting, and methodology of programming.

There are ten subtests for the High Speed Memory Board, each described individually. Details on interfacing to the Diagnostic Monitor are provided in the Diagnostic Monitor manual.

Early exit of each subtest is accomplished by depressing the stop key.

This series of tests assumes three other boards in the K105-D are functional. In addition to the MPU Board, required for basic operation, the Trace Control Board should be installed and operational. This board generates the link signal required by the High Speed Memory Board. The signal received is then checked to verify the signal is processed correctly by the High Speed Memory Board. The Clock/Threshold Board must be present so the probe thresholds can be varied. Finally, a high speed probe must be installed on the proper high speed input. The inputs must not be attached to either ground or any potential, but remain floating.

This series of subtests also assumes the board has passed the power up diagnostic. This diagnostic ensures most of the recording hardware as well as some memory functions correctly.

SUBTEST CATEGORIES

1. INTERNAL ARM CONTROL TEST
2. EXTERNAL ARM CONTROL TEST
3. TRIGGER TEST
4. LINK CONTROL TEST
5. CLOCK TEST
6. GLITCH DETECTION TEST
7. FILTER OPERATION TEST
8. DELAY COUNTER TEST
9. RAM DATA TEST
10. RAM ADDRESS TEST

ERROR COUNT CATEGORIES

1. Internal Arm Control Test Error Count

   A. Invalid Arm Trigger
   B. No Internal Arm Signal Detected

2. External Arm Control Test Error Count

   A. Invalid Arm Trigger
   B. No External Arm Signal Detected

3. Trigger Test Error Count

   A. No Trigger Found
   B. Invalid Trigger

4. Link Control Test Error Count

   A. No Internal Link Signal
   B. No External Link Signal

5. Clock Test Error Count

   A. No CPU Clock Error Count
   B. No Internal Clock
   C. No External Clock

6. Glitch Detection Test Error Count

   A. RAM Failure FF
   B. Glitch Detected During Sample Mode
   C. RAM Failure 00
   D. Glitch Not Detected During Glitch Mode

7. Filter Operation Test Error Count

   A. Triggered Immediately After Arming Error
   B. Early Trigger Error
   C. Trigger Never Occurred Error

8. Delay Counter Test Error Count

   A. Recording Ended Early Error
   B. Recording Never Ended
   C. Events Mode Ended Early
   D. Events Mode Never Ended

9. RAM Data Test Error Count: Memory Failure

10. RAM Address Test: Memory Addressing Failure

TITLE: INTERNAL ARM CONTROL TEST

PURPOSE: This subtest checks the arming control circuits.

TARGET HARDWARE: Chips located at 19A, 20A, and 20E.

DESCRIPTION: Using control and statusports, this subtest brings the hardware to a known state, arms the board for recording, and finally reads the armed line through a status port.

The following message is displayed throughout this test:

```
= TEST IN PROGRESS                    -STEP: ZZZ=
```

where ZZZ = 001 - 002

ERROR MESSAGE: Whenever an error is detected, one of the following messages is displayed:

```
=*TEST FAILED--                       -STEP: 001=
= INVALID ARM ERROR                           =

=*TEST FAILED--                       -STEP: 002=
= INTERNAL ARM SOURCE                         =
= DID NOT ARM ERROR                           =
```

TEST PASS: If the Arm Control Subtest encounters no errors, the following message is displayed:

```
= TEST PASSED                                 =
```

TITLE: EXTERNAL ARM CONTROL TEST

PURPOSE: This subtest tests the arming control circuits.

TARGET HARDWARE TESTED: Chips located at 19A, 20A, AND 20E

NOTE: This test requires the Trace Control Board to be present as signals generated by that board are required to exercise hardware.

DESCRIPTION: This subtest brings the hardware to a known state by writing to control ports, arms the board for recording by writing to a control port on the Trace Control board and finally reads the armed line through a status port.

The following message is displayed throughout this test:

```
= TEST IN PROGRESS                    -STEP: ZZZ=
```

where ZZZ = 001 - 003

ERROR MESSAGE: Whenever an error is detected, one of the following messages is displayed:

```
=*TEST FAILED--                       -STEP: 003=
= INVALID ARM ERROR                             =

=*TEST FAILED--                       -STEP: 003=
= NO EXTERNAL ARM ERROR                         =
= DID NOT ARM ERROR                             =
```

TEST PASS: If the Arm Control Subtest encounters no errors, the following message is displayed:

```
= TEST PASSED                                   =
```

TITLE: TRIGGER TEST

PURPOSE: This subtest exercises all the hardware in the trigger detector/ selector circuitry.

DESCRIPTION: This subtest brings the high-speed board to a known state, arms the board via control ports then uses self-test inputs and presents various data words to exercise the trigger. A successful trigger is based on the trigger true/false combinations which are set through control ports.

TARGET HARDWARE TESTED: Chips located at 20B, 20A, 19B, 14D, 5C, 5C, 6C, 5D, 6D, 6B, 7B, 8B

The patterns exercised are listed below:

STEP	DATAWORD	TRIG TRUE	TRIGGER FALSE
004		00000000B	00000000B
	00000000		
005	00000001		
006	00000010		
007	00000100		
008	00001000		
009	00010000		
010	00100000		
011	01000000		
012	10000000		
013		00000001B	00000000B
	00000000		
014	00000001		
015	00000010		
016	00000100		
017	00001000		
018	00010000		
019	00100000		
020	01000000		
021	10000000		
022		00000010B	00000000B
	00000000		
023	00000001		
024	00000010		
025	00000100		
026	00001000		
027	00010000		
028	00100000		
029	01000000		
030	10000000		
031		00000100B	00000000B
	00000000		
032	00000001		
033	00000010		
034	00000100		
035	00001000		

STEP	DATAWORD	TRIG TRUE	TRIGGER FALSE
036	00010000		
037	00100000		
038	01000000		
039	10000000		
040		00001000B	00000000B
	00000000		
041	00000001		
042	00000010		
043	00000100		
044	00001000		
045	00010000		
046	00100000		
047	01000000		
048	10000000		
049		00010000B	00000000B
	00000000		
050	00000001		
051	00000010		
052	00000100		
053	00001000		
054	00010000		
055	00100000		
056	01000000		
057	10000000		
058		00100000B	00000000B
	00000000		
059	00000001		
060	00000010		
061	00000100		
062	00001000		
063	00010000		
064	00100000		
065	01000000		
066	10000000		
067		01000000B	00000000B
	00000000		
068	00000001		
069	00000010		
070	00000100		
071	00001000		
072	00010000		
073	00100000		
074	01000000		
075	10000000		
076		10000000B	00000000B
	00000000		
077	00000001		
078	00000010		
079	00000100		
080	00001000		
081	00010000		
082	00100000		

STEP	DATAWORD	TRIG TRUE	TRIGGER FALSE
083	01000000		
084	10000000		
085		11111111B	11111111B
	11111111		
086	11111110		
087	11111101		
088	11111011		
089	11110111		
090	11101111		
091	11011111		
092	10111111		
093	01111111		
094		11111111B	11111110B
	11111111		
095	11111110		
096	11111101		
097	11111011		
098	11110111		
099	11101111		
100	11011111		
101	10111111		
102	01111111		
103		11111111B	11111101B
	11111111		
104	11111110		
105	11111101		
106	11111011		
107	11110111		
108	11101111		
109	11011111		
110	10111111		
111	01111111		
112		11111111B	11111011B
	11111111		
113	11111110		
114	11111101		
115	11111011		
116	11110111		
117	11101111		
118	11011111		
119	10111111		
120	01111111		
121		11111111B	11110111B
	11111111		
122	11111110		
123	11111101		
124	11111011		
125	11110111		
126	11101111		
127	11011111		
128	10111111		
129	01111111		

STEP	DATAWORD	TRIG TRUE	TRIGGER FALSE
130		11111111B	11101111B
	11111111		
131	11111110		
132	11111101		
133	11111011		
134	11110111		
135	11101111		
136	11011111		
137	10111111		
138	01111111		
139		11111111B	11011111B
	11111111		
140	11111110		
141	11111101		
142	11111011		
143	11110111		
144	11101111		
145	11011111		
146	10111111		
147	01111111		
148		11111111B	10111111B
	11111111		
149	11111110		
150	11111101		
151	11111011		
152	11110111		
153	11101111		
154	11011111		
155	10111111		
156	01111111		
157		11111111B	01111111B
	11111111		
158	11111110		
159	11111101		
160	11111011		
161	11110111		
162	11101111		
163	11011111		
164	10111111		
165	01111111		

166 FINAL TRIGGER TREE TEST

The following message is displayed throughout the test:

= TEST IN PROGRESS 3. TRIGGER TEST -STEP:ZZZ=

where ZZZ = 004 - 166

ERROR MESSAGE: Three error messages are generated by this subtest. The unit is tested for false as well as invalid triggers and then the final trigger

tree is tested. In the event of an error, one of the following messages is displayed:

```
=*TEST FAILED                              -STEP: ZZZ=
= TESTING TRIGGER XXXXX TREE                        =
= NO TRIGGER FOUND                                  =
= EXPECTED TRIGGER WAS = AA                         =
```

where

ZZZ is 004 - 165
XXXXX is either 'TRUE' or 'FALSE'
AAH is 00H - FFH

```
=*TEST FAILED                              -STEP: ZZZ=
= TESTING TRIGGER XXXXX TREE                        =
= INVALID TRIGGER OCCURRED                          =
= EXPECTED TRIGGER WAS AAH                          =
= TRIGGERED ON = BBH                                =
```

where

ZZZ is 004 - 165
XXXXX is either 'TRUE' or 'FALSE'
AAH is 00H - FFH

The above tests use the Not Triggers Output (IC 8B PIN 15) in the status port to determine if the Trigger True and Trigger False parameters function correctly. The following test checks the Final Triggered output (1C, 17A, PIN 3). The Final Triggered Output (IC 17A PIN 3). If an error exists in this data path, the following error message is displayed.

```
=*TEST FAILED                              -STEP: 166=
= TESTING FINAL TRIGGER TREE                        =
= FINAL TRIGGER TREE FAILURE                        =
```

TEST PASSED: In the event that no errors are detected, the following message is displayed:

```
= TEST PASSED                                       =
```

TITLE: LINK CONTROL TEST

PURPOSE: This subtest verifies that during link mode operation, the recording does not occur until triggered by a signal from the Trace Control Board. During non-link, the recording occurs when the high speed triggering inputs meet the qualification test.

TARGET HARDWARE TESTED: Chips located at 19B, 20C

NOTE: This test requires the Trace Control Board to be present, as signals generated by that board are required to exercise the hardware.

DESCRIPTION: This subtest verifies that the link signal on the ink signal from the Trace Control Board reaches the High-Speed board. This signal is detected by reading a status port.

The following message is displayed throughout the test:

```
= TEST IN PROGRESS: 4. LINK CONTROL     -STEP: ZZZ=

                where ZZZ = 167  - 168
```

ERROR MESSAGE: Whenever an error is detected, one of the following messages is displayed:

```
= TEST FAILED--                         -STEP: 167=
= INVALID LINK CONDITION                        =

=*TEST FAILED--                         -STEP: 168=
= NO LINK SIGNAL RECEIVED                       =
```

TEST PASS: If the UUT completes this subtest without encountering any errors, the following message is displayed:

```
= TEST PASSED                                   =
```

TITLE: CLOCK TEST

PURPOSE: This subtest verifies operation of the Main Trigger/ Clock Circuit in both internal and external modes.

TARGET HARDWARE TESTED: Chips located at 6A, 8A, 9A, 10A, 11A, 12A

DESCRIPTION: This subtest exercises each of the following inputs to the Clock Selector Circuit:

A. CPU CLOCK
B. INTERNAL CLOCK (FROM CLOCK THRESHOLD)
C. EXT CLOCK INPUT (PROBES)

Each of the clocks is individually selected and the status is read to determine if the given clock has caused a trigger.

The following message is displayed throughout the test.

```
= TEST IN PROGRESS-- 5. CLOCK TEST       -STEP: ZZZ=

                where ZZZ = 169 - 174
```

ERROR MESSAGE: Whenever an error is detected, one of the following error messages is displayed:

```
=*TEST FAILED                                -STEP: 169=
= NO TRIGGER AFTER USING CPU CLOCK                    =

=*TEST FAILED                                -STEP: 170=
= NO TRIGGER AFTER USING INTERNAL CLOCK               =

=*TEST FAILED                                -STEP: ZZZ=
= EXTERNAL CLOCK TEST                                 =
= SECK LINE SELECTED                                  =
= YYYY LINE = X                                       =
= NO TRIGGER AFTER USING EXTERNAL CLOCK               =

     where ZZZ is 171,172
           X   is 0,1
          YYYY is CKTF,CQTF

=*TEST FAILED                                -STEP: ZZZ=
= EXTERNAL CLOCK TEST                                 =
= SECQ LINE SELECTED                                  =
= YYYY LINE = X                                       =
= NO TRIGGER AFTER USING EXTERNAL CLOCK               =

     where ZZZ is 173,174
           X   is 0,1
          YYYY is CKTF,CQTF
```

```
        =*TEST FAILED                                   -STEP: ZZZ=
        = EXTERNAL CLOCK TEST                                   =

= SECK LINE SELECTED                                    =
        = YYYY LINE = X                                         =
        = CLOCKED ON INCORRECT EDGE                             =

             where ZZZ is 171,172
                   X   is 0,1
                  YYYY is CKTF,CQTF

        =*TEST FAILED                                   -STEP: ZZZ=
        = EXTERNAL CLOCK TEST                                   =
        = SECQ LINE SELECTED                                    =
        = YYYY LINE = X                                         =
        = CLOCKED ON INCORRECT EDGE                             =

             where ZZZ is 173,174
                   X   is 0,1
                  YYYY is CKTF,CQTF
```

TEST PASS: If the UUT performs a complete pass through this routine without encountering any errors, the following message is displayed:

```
      = TEST PASSED                                             =
```

TITLE: GLITCH DETECTION TEST

PURPOSE: This subtest Verifies operation of the Glitch/Sample circuit through the use of the high speed probes; the probes must be attached to the unit for this test to run properly.

TARGET HARDWARE TESTED: Chips located at 1C, 2C, 3C, 4C, 1D, 2D, 3D, 4D, 1E, 2E, 3E, 4E 1A, 2A, 4A, 5A, 1B, 2B, 3B, 4B

DESCRIPTION: The probes are used to force a logic 1/0 into the input data path. Various modes are set, and glitches simulated, and checked if detected. The following message is displayed throughout the test:

```
= TEST IN PROGRESS: 6. GLITCH TEST        STEP:ZZZ=

                where ZZZ = 175 - 178
```

ERROR MESSAGE: This subtest assumes that one can read and write fairly reliably to the high speed memory, as the only way to read the contents of the datapath is to pipeline the information through the RAMs. If the zero written through the datapath cannot be read out through the RAMs, the following error message is displayed:

```
=*TEST FAILED--                              -STEP: 175=
= DATA LOADED THROUGH PROBES                           =
= CPU CLOCK SELECTED                                   =
= HS RAM FAILURE                                       =
= BASE ADDRESS = 0000H                                 =
= DATA WRITTEN = FFH                                   =
= DATA READ    = CCH                                   =

     where CC is 0-FF

=*TEST FAILED--                              -STEP: 176=
= GLITCH DETECTED DURING SAMPLE MODE                   =
= EXPECTED VALUE = 00H                                 =
= ACTUAL VALUE   = BBH                                 =

     where BB is 0-FF

=*TEST FAILED--                              -STEP: 177=
= DATA LOADED THROUGH PROBES                           =
= CPU CLOCK SELECTED                                   =
= HS RAM FAILURE                                       =
= BASE ADDRESS = 0000H                                 =
= DATA WRITTEN = 00H                                   =
= DATA READ    = AAH                                   =

     where AA is 0 TO FFH
```

```
=*TEST FAILED--                                  -STEP: 178=
= GLITCH NOT DETECTED                                    =
= EXPECTED SET VALUE          =FFH                       =
= ACTUAL SET VALUE            =AAH                       =
= EXPECTED RESET VALUE        =00H                       =
= ACTUAL RESET VALUE          =BBH                       =

     where AA is 0-FF
           BB is 0-FF
```

TEST PASS: If all testing is completed without error, the following message is displayed:

```
= TEST PASSED                                            =
```

TITLE: FILTER OPERATION TEST

PURPOSE: Tests the Filter Counter.

DESCRIPTION: This subtest exercises the Filter Counter Circuits by setting a value and then allowing the qualifying trigger word to occur the specified amount of times. Checking is performed before, during and after the specified amount of qualifying triggers has occurred.

TARGET HARDWARE TESTED: Chips located at 11A, 14A, 17A, 18A, 19B, 19C

Filter values are set as shown below:

TEST STEP NUMBER	FILTER VALUE
179	1H
180	2H
181	3H
182	4H
183	5H
184	6H
185	7H
186	8H
187	9H
188	AH
189	BH
190	CH
191	DH
192	EH

= TEST IN PROGRESS: 7. FILTER TEST -STEP: ZZZ=

where ZZZ is 179 - 192

ERROR MESSAGE: If memory read does not match the pattern written, the following error message is displayed:

```
=*TEST FAILED--                          -STEP: ZZZ=
=HS RAM FAILURE                                  =
=EXPECTED VALUE = WWH                            =
=READ VALUE     = RRH                            =
=CLOCK COUNT    = XXXH                           =
```

where ZZZ is 225 - 238
XXX should be 0-3FF
WW should be 0-FF
RR should be 0-FF

Each time the failure sequence is entered, the total error count and the subtest error count is incremented.

TEST PASS: If the data read matches the data written, the follow-ing message is displayed.

```
      = TEST PASSED                                    =
```

TITLE: DELAY COUNTER TEST

PURPOSE: This subtest verifies the recording stops properly based on the delay counter expiring. this test also confirms operation of the 16-bit up counter.

TARGET LOGIC: 13A, 15A, 14B, 15B, 16B, 17B, 18B

DESCRIPTION: This subtest checks the delay counter circuitry by exercising the counter using all significant bits as shown in the following pattern:

Test Step #	Delay Data Pattern	
The following is performed with clock mode selected:		
193	0000000000000001b	0001h
194	0000000000000010b	0002h
195	0000000000000100b	0004h
196	0000000000001000b	0008h
197	0000000000010000b	0010h
198	0000000000100000b	0020h
199	0000000001000000b	0040h
200	0000000010000000b	0080h
201	0000000100000000b	0100h
202	0000001000000000b	0200h
203	0000010000000000b	0400h
204	0000100000000000b	0800h
205	0001000000000000b	1000h
206	0010000000000000b	2000h
207	0100000000000000b	4000h
208	1000000000000000b	8000h
The following is performed with event mode selected:		
209	0000000000000001b	0001h
210	0000000000000010b	0002h
211	0000000000000100b	0004h
212	0000000000001000b	0008h
213	0000000000010000b	0010h
214	0000000000100000b	0020h
215	0000000001000000b	0040h
216	0000000010000000b	0080h
217	0000000100000000b	0100h
218	0000001000000000b	0200h
219	0000010000000000b	0400h
220	0000100000000000b	0800h
221	0001000000000000b	1000h
222	0010000000000000b	2000h
223	0100000000000000b	4000h
224	1000000000000000b	8000h

The following message is displayed throughout this test:

```
================================================
= Test in progress:8. Delay counter test-step: zzz=
================================================
```

where zzz should be 193 - 224

ERROR MESSAGE: In the event the recording either never ends or ends before the expected delay count is reached, one of the following messages is displayed:

```
================================================
=*Test failed--                          -step: zzz=
= Recording ended early!                          =
= Expected delay count = aaaah                    =
= Actual delay count   = bbbbh                    =
================================================

================================================
=*Test failed--                          -step: zzz=
= Recording never ended!                          =
= Expected delay count = aaaah                    =
================================================
```

where zzz is steps 193 - 224
aaaa is 0000h-ffffh
bbbb is 0000h-ffffh

Test Pass: If the count matches all data patterns the following message is displayed:

```
================================================
= Test Passed                                     =
================================================
```

TITLE: RAM DATA TEST

PURPOSE: This subtest verifies operation of the 8 RAM memories by clocking (through CPU self-test inputs) into the data path a data pattern. The pattern is then read back and compared until all RAM is written to.

TARGET LOGIC: 9E, 9B, 11E, 11B, 10E, 10B, 12E, 12B

DESCRIPTION: RAM is set up as split memory and is not directly accessible. All input to memory must come from either the k105-D high speed probes or the CPU self-test inputs. Data must be transferred into memory in a serial type mode. The characteristics of this subtest are as follows:

Test step #	Data Byte Pattern
225	00H
226	aaH
227	55H
228	ccH
229	33H
230	01H
231	02H
232	04H
233	08H
234	10H
235	20H
236	40H
237	80H
238	ffH

The following message is displayed throughout this test:

```
=================================================
= Test in progress: 9. RAM Data Integrity-step:  zzz=
=================================================
```

where zzz should be 225 - 238

ERROR MESSAGE: If memory read does not match the pattern written, the following error message is displayed:

```
=================================================
=*Test Failed--                          -Step: ZZZ=
=HS RAM Failure                                    =
=Expected Value = WWH                              =
=Read Value     = RRH                              =
=Clock Count    = XXXH                             =
=================================================
```

```
where zzz is 225 - 238
      xxx should be 0-3ff
      ww  should be 0-ff
      rr  should be 0-ff
```

Each time the failure sequence is entered the total error count and the subtest error count is incremented.

Test Pass: If the data read matches the data written, the following message is displayed.

```
================================================
= Test Passed                                  =
================================================
```

TITLE: RAM ADDRESS TEST

PURPOSE: The purpose of this subtest is to selectively write into only one memory component at a time and verify that chip is the only memory device accessed.

TARGET HARDWARE TESTED: Chips located AT 9C, 12C, 13C, 9D, 12D

DESCRIPTION: This subtest is accomplished by zeroing out the entire memory and then writing a pattern into one of 4 blocks as described below. The entire memory array is then read and compared with the pattern written.

The characteristics of the subtest are as follows:

The 1K of HS RAM can best be thought of as divided into four, 256 byte sections.

TEST STEP #	PATTERN WRITTEN
239	1,0,0,0,2,0,0,0...255,0,0,0
240	0,1,0,0,0,2,0,0...0,255,0,0
241	0,0,1,0,0,0,2,0...0,0,255,0
242	0,0,0,1,0,0,0,2...0,0,0,255

LOOP ON ERROR: Note that in this subtest, Loop On Error functions slightly differently than in other tests. If Loop On Error is set and an error is encountered, the program continues to check RAM until clock count reaches 03FFH. At this point, the RAM is rewritten with the same pattern as when the error was encountered. Therefore, it is possible for the clock count to increase even if Loop On Error is set.

The following message is displayed throughout the test:

```
= TEST IN PROGRESS: 10. RAM ADDRESS TEST  -STEP: ZZZ=
```

where ZZZ should be ??-??

ERROR MESSAGE: Whenever the data pattern read is found to be other than the data asserted, the following error message is displayed:

```
=*TEST FAILED--                          -STEP: ZZZ=
= HS RAM ADDRESS TEST                             =
= EXPECTED VALUE = AAH                            =
= READ VALUE     = BBH                            =
= CLOCK COUNT    = CCCCH                          =
```

where ZZZ is 239 - 242
AA is 00 - FF
BB is 00 - FF
CCCC is 0000 - 3FFF

If this error occurs, the total error count and subtest error count should be incremented.

TEST PASS: If no error occurs, the following message is displayed:

```
= TEST PASSED                                    =
```

OVERVIEW

This section describes the subtests executed on the K105-D I/O board, and the associated error reporting and methodology of programming.

The I/O board diagnostic is divided into twelve subtests, each of which is described individually on the following pages.

Subtest 1 is an EPROMS Checksum Test; subtests 2 and 3 are RAM Data and Address Integrity Tests; subtests 4 and 5 are Serial I/O Port #1 and #2 tests; subtests 6 through subtest 9 are Floppy Disk Controller tests; the DMA operation is incorporated in subtests 7 through subtest 9 for data transfer; subtest 10 is an 8253 counter 0 test; and subtests 11 through subtest 12 are GPIB tests.

Subtest 4 and 5 need an RS-232 wrap back connector to perform the test.

Subtest 11 and 12 are GPIB tests. First the operator should get one system diskette for 9520 CP/M along with GPIBC.COM file. Then the operator should run GPIB controller software under 9520 before proceeding.

NOTE: 1. The °TARGET LOGIC' listed in each subtest description does not necessarily include all of the logic which could affect the operation of that subtest.

2. The IC locations given in this chapter are accurate for a particular rev level in the board. Since the rev level may differ, the reader should remember that the IC locations given here are dependent upon the schematic.

SUBTEST CATEGORIES

1. ROM CHECKSUM TEST
2. RAM DATA TEST
3. RAM ADDRESS TEST
4. SERIAL I/O PORT #1 TEST
5. SERIAL I/O PORT #2 TEST
6. FDC SEEK TRACK TEST
7. FDC FIXED PATTERN TEST
8. FDC/DMA ADDRESS TEST
9. FDC RANDOM WRITE/READ TEST
10. 8253 COUNTER 0 TEST

ERROR COUNT CATEGORIES

1. SUBTEST 1 ERROR COUNT
2. SUBTEST 2 ERROR COUNT
3. SUBTEST 3 ERROR COUNT
4. SUBTEST 4 ERROR COUNT
5. SUBTEST 5 ERROR COUNT
6. SUBTEST 6 ERROR COUNT
7. SUBTEST 7 ERROR COUNT
8. SUBTEST 8 ERROR COUNT
9. SUBTEST 9 ERROR COUNT
10. SEEK COMMAND ERROR COUNT
11. RECALIBRATE COMMAND ERROR COUNT
12. WRITE SECTOR COMMAND ERROR COUNT
13. READ SECTOR COMMAND ERROR COUNT
14. DRIVE A ERROR COUNT
15. DRIVE B ERROR COUNT
16. SIDE 0 ERROR COUNT
17. SIDE 1 ERROR COUNT
18. SOFT ERROR COUNT
19. HARD ERROR COUNT
20. NOT READY ERROR COUNT
21. WRITE PROTECT ERROR COUNT
22. ABNORMAL TERMINATION ERROR COUNT
23. FDC BAD DATA ERROR COUNT
24. SUBTEST 10 ERROR COUNT
25. SUBTEST 11 ERROR COUNT
26. SUBTEST 12 ERROR COUNT

TITLE: ROM CHECKSUM TEST

TARGET LOGIC: 17C, 17D, 18C, 18D, 17B, 18B, 10C, 11.5D, 14C, 14D, 13C, and MPU memory read logic

DESCRIPTION: The ROM Checksum Test is functionally tested by reading the content of each EPROM location, summing up through all 8K locations, and then comparing the read checksum to the expected checksum for verification.

The following table indicates the EPROM being tested for the various diagnostic steps.

TEST STEP	LOCATION	STARTING ADDRESS	END ADDRESS	A0
1	17C	68000H	69FFEH	0(EVEN)
2	17D	68001H	69FFFH	1(ODD)
3	18C	6C000H	6DFFEH	0(EVEN)
4	18D	6C001H	6DFFFH	1(ODD)

ERROR MESSAGE:

If an error occurs, the following message is displayed:

*TEST FAILED--TEST STEP zzz
ROM CHECKSUM CALCULATION
EPROM ADDRESS=6xxxxH
CALCULATED CHECKSUM=ssssH
EXPECTED CHECKSUM=eeeeH

where zzz should be 1 through 4
xxxx should be 8000, 8001, C000, C001
ssss should be 0000 through FFFF
eeee should be 0000 through FFFF

TITLE: RAM DATA INTEGRITY TEST

TARGET LOGIC: 15C, 15D, 16C, 16D, 17B, 18B, 10C, 11.5D, 14C, 14D, 13C and MPU memory write/read logic

DESCRIPTION: The RAM Data Integrity Test is functionally tested by writing the Word Data Pattern into the word location and immediately reading back the word data of this location. It is then verified by comparing the word data read to the word data written.

The RAM location range of the I/O option board is from 60000H through 60FFFH and 64000H through 64FFFH. The range from 61000H through 63FFFH is skipped.

The following table indicates the data being tested for the various diagnostic steps.

TEST STEP	DATA WORD PATTERN
5	0AAAAH
6	05555H
7	0CCCCH
8	03333H
9	0001H
10	0002H
11	0004H
12	0008H
13	0010H
14	0020H
15	0040H
16	0080H
17	0100H
18	0200H
19	0400H
20	0800H
21	1000H
22	2000H
23	4000H
24	8000H

ERROR MESSAGE:
If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP    zzz
ADDRESS = 6xxxxH
DATA WRITTEN = wwwwH
DATA READ    = rrrrH

where zzz should be 5 through 24
xxxx should be 0000 through 0FFF AND 4000 through 4FFF
wwww should be AAAA, 5555, CCCC, 3333,
                     0001, 0002, 0004, 0008,
                     0010, 0020, 0040, 0080,
                     0100, 0200, 0400, 0800,
                     1000, 2000, 4000, 8000, and
rrrr should be 0000 through FFFF
```

TITLE: RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 15C, 15D, 16C, 16D, 17B, 18B, 10C, 11.5D, 14C, 14D, 13C and MPU memory write/read logic

DESCRIPTION: The RAM Address Integrity is functionally tested by writing word data pattern 0AAAAH into the asserted location, then reading other locations. The address integrity is then verified by comparing the word data read to the pattern 0AAAAH.

The RAM location range of I/O option board is from 60000H through 60FFFH and 64000H through 64FFFH. The range from 61000H through 63FFFH is skipped.

The following table indicates the asserted address bit being tested for the various diagnostic steps:

TEST STEP	ADDRESS LINE ASSERTED	DATA WORD PATTERN
25	A00(60001H)	0AAAAH
26	A01(60002H)	0AAAAH
27	A02(60004H)	0AAAAH
28	A03(60008H)	0AAAAH
29	A04(60010H)	0AAAAH
30	A05(60020H)	0AAAAH
31	A06(60040H)	0AAAAH
32	A07(60080H)	0AAAAH
33	A08(60100H)	0AAAAH
34	A09(60200H)	0AAAAH
35	A10(60400H)	0AAAAH
36	A11(60800H)	0AAAAH
37	A12(64000H)	0AAAAH

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
WROTE TO ADDRESS 6wwwwH
DATA =ddddH
FOUND AT ADDRESS 6aaaaH

where zzz should be 25 through 37
wwww should be 0000 through 0FFF AND 4000 through 4FFF
dddd should be AAAA
aaaa should be 0000 through 0FFF AND 4000 through 4FFF
```

TITLE: SERIAL I/O PORT #1 TEST

TARGET LOGIC: 5B, 4B, 10D, 13C, 13D, 7C, 7D, 5A, 4A

DESCRIPTION: Serial I/O Port #1 is functionally tested by using USART #1 as a transmitter and receiver and transmitting the 8 bit data patterns and receiving the transmitted bytes through the wrap back RS-232 connector within a specified time window (95% through 105%).

If the RS-232 wrap back connector is attached to the back panel, it should be configured as follows:

pin 2 short to pin 3,
pin 4 short to pin 5,
pin 6 short to pin 20.

If the wrap back connector is attached to the I/O option board J2, it should be configured as follows:

pin 1 short to pin 3,
pin 5 short to pin 7,
pin 9 short to pin 12.

The following patterns are then transmitted: 0AAH, 55H, 0CCH, 33H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

The following baud rates are tested: 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600.

The following table indicates the baud rates and byte patterns being tested for the various diagnostic steps.

TEST STEP	BAUD RATE	DATA PATTERN
38-49	110	0AAH,155H,20CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
50-61	150	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
62-73	300	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
74-85	600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
86-97	1200	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
98-109	1800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
110-121	2400	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
122-133	4800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
134-145	9600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:

1. If an error of Transmitter Buffer Not Empty occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
SERIAL PORT 1
bbbb BAUD
TRANSMITTER BUFFER NOT EMPTY
STATUS READ TXRDY IS NOT TRUE
STATUS READ TXE IS NOT TRUE

where zzz should be 38 through 145 and
bbbb should be 110, 150, 300, 600, 1200,
              1800, 2400, 4800, or 9600.
```

2. If an error of No Character Received occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
SERIAL PORT 1
bbbb BAUD
NO CHARACTER RECEIVED
STATUS READ DSR IS NOT TRUE
STATUS READ RXRDY IS NOT TRUE

where zzz should be 38 through 145 and
bbbb should be 110, 150, 300, 600, 1200,
              1800, 2400, 4800, or 9600.
```

3. If an error of Character Received Early occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
SERIAL PORT 1
bbbb BAUD
CHARACTER RECEIVED EARLY
SOFTWARE COUNT=ccccH
EXPECTED COUNT=eeeeH

where zzz should be 38 through 145
bbbb should be 110, 150, 300, 600, 1200,
              1800, 2400, 4800, or 9600.
cccc should be 1 through FFFF
eeee  should be 95% expected count of each baud rate
```

4. If an error of Character Received Late occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
SERIAL PORT 1
bbbb BAUD
CHARACTER RECEIVED LATE
SOFTWARE COUNT=ccccH
EXPECTED COUNT=eeeeH
```

where zzz should be 38 through 145
bbbb should be 110, 150, 300, 600, 1200,
1800, 2400, 4800, or 9600.
cccc should be 1 through FFFF
eeee should be 105% expected count of each baud rate

5. If an error of Bad Data occurs, the following message is displayed:

*TEST FAILED--TEST STEP zzz
SERIAL PORT 1
bbbb BAUD
DATA RECEIVED=rrH
DATA S/B=ttH

where zzz should be 38 through 145
bbbb should be 110, 150, 300, 600, 1200,
1800, 2400, 4800, or 9600.
rr should be 00 through FF
tt should be 0AAH, 55H, 0CCH, 33H, 01H, 02H, 04H, 08H

TITLE: SERIAL I/O PORT #2 TEST

TARGET LOGIC: 6B, 4B, 10D, 13C, 13D, 7C, 7D, 7A, 6A

DESCRIPTION: Serial I/O Port #2 is functionally tested by using USART #2 as a transmitter and receiver and transmitting the 8 bit data patterns and receiving the transmitted bytes through the wrap back RS-232 connector within a specified time window(95% through 105%).

If the RS-232 wrap back connector is attached to the back panel, it should be configured as follows:

pin 2 short to pin 3,
pin 4 short to pin 5,
pin 6 short to pin 20.

If the wrap back connector is attached to the I/O option board J3, it should be configured as follows:

pin 1 short to pin 3,
pin 5 short to pin 7,
pin 9 short to pin 12.

The following patterns are transmitted: 0AAH, 55H, 0CCH, 33H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

The following baud rates are tested: 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600.

The following table indicates the baud rates and byte patterns being tested for the various diagnostic steps.

TEST STEP	BAUD RATE	DATA PATTERN
146 through 157	110	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
158 through 169	150	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
170 through 181	300	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
182 through 193	600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
194 through 205	1200	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
206 through 217	1800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
218 through 229	2400	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
230 through 241	4800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
242 through 253	9600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:

1. If an error of Transmitter Buffer Not Empty occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
SERIAL PORT 2
bbbb BAUD
TRANSMITTER BUFFER NOT EMPTY
STATUS READ TXRDY IS NOT TRUE
STATUS READ TXE IS NOT TRUE

where zzz should be 146 through 253
bbbb should be 110, 150, 300, 600, 1200,
               1800, 2400, 4800, or 9600.
```

2. If an error of No Character Received occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
SERIAL PORT 2
bbbb BAUD
NO CHARACTER RECEIVED
STATUS READ DSR IS NOT TRUE
STATUS READ RXRDY IS NOT TRUE

where zzz should be 146 through 253
bbbb should be 110, 150, 300, 600, 1200,
               1800, 2400, 4800, or 9600.
```

3. If an error of Character Received Early occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
SERIAL PORT 2
bbbb BAUD
CHARACTER RECEIVED EARLY
SOFTWARE COUNT=ccccH
EXPECTED COUNT=eeeeH

where zzz should be 146 through 253
bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600
cccc should be 1 through FFFF
eeee  should be 95% expected count of each baud rate
```

4. If an error of Character Received Late occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
SERIAL PORT 2
bbbb BAUD
CHARACTER RECEIVED LATE
SOFTWARE COUNT=ccccH
EXPECTED COUNT=eeeeH

where zzz should be 146 through 253
bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600
```

```
cccc should be 1 through FFFF
eeee  should be 105% expected count of each  baud
      rate
```

5. If an error of Bad Data occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
SERIAL PORT 2
bbbb BAUD
DATA RECEIVED=rrH
DATA S/B=ttH

where zzz should be 146 through 253
bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600
rr should be 00 through FF
tt should be 0AAH, 55H, 0CCH, 33H, 01H, 02H, 04H, 08H
```

TITLE: FDC SEEK TRACK TEST

TARGET LOGIC: 3C, 3D, 1D, 2D, 4D, 2B.2C, 1C, 1A, 1B, 3B, 2A and disk driver logic

DESCRIPTION: The FDC Seek Track Test is functionally tested by seeking the desired track using 3 methods:

1. Seek next track from low track to high track (track 0 to track 39).
2. Seek next track from high track to low track (track 39 to track 0).
3. Seek spirally, from track 0 to 39, 39 to 1, 1 to 38 until middle track (track 20) is found

The following table indicates the drive, side, and disk operation for the various diagnostic test steps:

TEST STEP	DRIVE	SIDE	DISK OPERATION
254	A	0	SENSE DRIVE READY
255	A	0	RETRACK TO 0
256	A	0	LOW-->HIGH SEEK
257	A	0	HIGH-->LOW SEEK
258	A	0	SPIRAL SEEK
259	A	1	SENSE DRIVE READY
260	A	1	RETRACK TO 0
261	A	1	LOW-->HIGH SEEK
262	A	1	HIGH-->LOW SEEK
263	A	1	SPIRAL SEEK
264	B	0	SENSE DRIVE READY
265	B	0	RETRACK TO 0
266	B	0	LOW-->HIGH SEEK
267	B	0	HIGH-->LOW SEEK
268	B	0	SPIRAL SEEK
269	B	1	SENSE DRIVE READY
270	B	1	RETRACK TO 0
271	B	1	LOW-->HIGH SEEK
272	B	1	HIGH-->LOW SEEK
273	B	1	SPIRAL SEEK

ERROR MESSAGE:

1. If an error of Sense Drive Status Command Error occurs, the following message is displayed:

   FDD NOT READY

   Afterwards the diagnostic will retry ten times. To get the operator's attention in case of not a real error, the following message is displayed:

   *TEST FAILED--TEST STEP zzz
   COMMAND RETRYING COUNT DOWN yy TIMES
   FDD NOT READY

   where zzz should be 254, 259, 264, 269
   yy should be 1 through 9

2. If an error of Recalibrate Command occurs, the following message is displayed:

   *TEST FAILED--TEST STEP zzz
   FDD EQUIPMENT CHECK
   ABNORMAL TERMINATION
   INVALID COMMAND
   FDD READY CHANGE
   SEEK ERROR

   where zzz should be 255, 260, 265, 270.
   One or more of the lightface message lines will appear depending on whether or not that kind of error occurs.

3. If an error of Seek And Verify Task occurs, the following message is displayed:

   *TEST FAILED TEST STEP zzz
   ABNORMAL TERMINATION
   INVALID COMMAND
   FDD READY CHANGE
   SEEK ERROR
   SEEK COMMAND
   DRIVE d SIDE s
   TRACK WAS ON ttt
   TRACK S/B ON ccc

   where zzz should be 256, 257, 258, 261, 262,
   263, 266, 267, 268, 271, 272, 273
   d SHOULD BE A OR B
   s SHOULD BE 0 OR 1
   ttt SHOULD BE 0 40
   ccc SHOULD BE 0 40

   One or more of the lightface message lines will appear on the screen depending on whether or not that kind of error occurs.

TITLE: FDC FIXED PATTERN TEST

TARGET LOGIC: 3C, 3D, 1D, 2D, 4D, 2B.2C, 1C, 1A, 1B, 3B, 2A, 13B, 12B, 12A, 11B, 9A, 9B and disk driver logic.

DESCRIPTION: The FDC Fixed Pattern Test is functionally tested by using DMA data transfer, writing sector 512 fixed pattern bytes, reading the sector back, and comparing the Read Buffer with the Write Buffer.

The 512 fixed pattern bytes will be arranged as 0DBH, 06BH, 14H, 94H a data pack; thus each sector has 512/4=128 packs. It is necessary to verify that all 40 tracks each have eight sectors and that each sector has 512 bytes.

The following table indicates the drive, side, disk operation and data pattern being tested for the various diagnostic test steps:

TEST STEP	DRIVE	SIDE	DISK OPERATION	DATA PATTERN
274	A	0	SENSE DRIVE READY	NONE
275	A	0	RETRACK TO 0	NONE
276	A	0	SECTOR W/R/VERIFY	0DBH, 6BH, 14H, 94H
277	A	1	SENSE DRIVE READY	NONE
278	A	1	RETRACK TO 0	NONE
279	A	1	SECTOR W/R/VERIFY	0DBH, 6BH, 14H, 94H
280	B	0	SENSE DRIVE READY	NONE
281	B	0	RETRACK TO 0	NONE
282	B	0	SECTOR W/R/VERIFY	0DBH, 6BH, 14H, 94H
283	B	1	SENSE DRIVE READY	NONE
284	B	1	RETRACK TO 0	NONE
285	B	1	SECTOR W/R/VERIFY	0DBH, 6BH, 14H, 94H

ERROR MESSAGE:

1. If an error of Sense Drive Status Command error occurs, the following message is displayed:

   *TEST FAILED--TEST STEP zzz
   FDD NOT READY

   Afterwards, the diagnostic will retry 10 times. To get the operator's attention in the event it is not a real error, the following message is displayed:

   *TEST FAILED--TEST STEP zzz
   COMMAND RETRYING COUNT DOWN yy TIMES
   FDD NOT READY

   where zzz should be 274, 277, 280, 283
   yy should be 1 through 9

2. If an error of Recalibrate Command occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
FDD EQUIPMENT CHECK
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
SEEK ERROR
```

where zzz should be 275, 278, 281, 284

The error message lines printed above in lightface type will appear on the screen depending on whether or not this kind of error occurs.

3. If an error of Write Sector Command occurs, the following is displayed:

```
*TEST FAILED--TEST STEP   zzz
WRITE SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY
```

where zzz should be 276, 279, 282, 285
d should be A OR B
s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7

The error message lines printed above in lightface type will appear on the screen depending on whether or not this kind of error occurs.

After the very first error, the operation will retry 10 times, and the following message will be displayed afterwards:

```
*TEST FAILED--TEST STEP   zzz
COMMAND RETRYING COUNT DOWN yy TIMES
WRITE SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
```

```
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY
```

where yy should be 1 through 9
zzz should be 276, 279, 282, 285
d should be A OR B
s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7

The error message lines printed above in lightface type will appear on the screen depending on whether or not this kind of error occurs.

4. If an error of Read Sector Command occurs, the following is displayed:

```
*TEST FAILED--TEST STEP   zzz
READ SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY
```

where zzz should be 276, 279, 282, 285
d should be A OR B
s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7

The error message lines printed above in lightface type

will appear on the screen depending on whether or not this kind of error occurs. After the very first error, the operation will retry 10 times, and the following message will be displayed afterwards:

```
*TEST FAILED--TEST STEP   zzz
COMMAND RETRYING COUNT DOWN yy TIMES
READ SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY
```

where yy should be 1 through 9
zzz should be 276, 279, 282, 285
d should be A OR B
s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7

The error message lines printed above in lightface type will appear on the screen depending on whether or not this kind of error occurs.

5. If an error of Bad Sector Data occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
READ SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FAILED AT BYTE NUMBER nnnH
EXPECTED DATA=eeH
DATA READ=xxH
```

where zzz should be 276 through 287, 290 through 301, 304 through 315, 318 through 329
d should be A OR B
s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7
nnn should be 000-200
ee should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80
xx should be 00 through FF

TITLE: FDC/DMA ADDRESS TEST

TARGET LOGIC: 3C, 3D, 1D, 2D, 4D, 2B.2C, 1C, 1A, 1B, 3B, 2A, 13B, 12B, 12A, 11B, 9A, 9B and disk driver logic.

DESCRIPTION: The FDC/DMA Address Integrity is functionally tested by writing 512 bytes 0AAH into a random sector of a random track, then using DMA read operation to read the whole sector data back to the asserted address buffer. The address integrity is then verified by comparing the Write Buffer and the Read Buffer.

The drive and side are defaulted to drive B, side 0. If drive B is not selected, then drive A side 0 is selected.

The asserted address lines are A00 through A11, and A14 to which the RAM address in the I/O option board is assigned.

The following table indicates the drive, side, disk operation, address bit asserted being tested for the various diagnostic test steps:

TEST STEP	DRIVE	SIDE	DISK OPERATION	ADDRESS BIT ASSERTED
286	A OR B	0 OR 1	SENSE DRIVE READY	NONE
287	A OR B	0 OR 1	RETRACK TO 0	NONE
288	A OR B	0 OR 1	SECTOR W/R/VERIFY	A00
289	A OR B	0 OR 1	SECTOR W/R/VERIFY	A01
290	A OR B	0 OR 1	SECTOR W/R/VERIFY	A02
291	A OR B	0 OR 1	SECTOR W/R/VERIFY	A03
292	A OR B	0 OR 1	SECTOR W/R/VERIFY	A04
293	A OR B	0 OR 1	SECTOR W/R/VERIFY	A05
294	A OR B	0 OR 1	SECTOR W/R/VERIFY	A06
295	A OR B	0 OR 1	SECTOR W/R/VERIFY	A07
296	A OR B	0 OR 1	SECTOR W/R/VERIFY	A08
297	A OR B	0 OR 1	SECTOR W/R/VERIFY	A09
298	A OR B	0 OR 1	SECTOR W/R/VERIFY	A10
299	A OR B	0 OR 1	SECTOR W/R/VERIFY	A11
300	A OR B	0 OR 1	SECTOR W/R/VERIFY	A14

ERROR MESSAGE:

1. If an error of Sense Drive Status Command error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
FDD NOT READY
```

Afterwards, the diagnostic will retry 10 times. To get the operator's attention in the event that there is not a real error, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
COMMAND RETRYING COUNT DOWN yy TIMES
FDD NOT READY
```

where zzz should be 286
yy should be 1 through 9

2. If an error of Recalibrate Command occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
FDD EQUIPMENT CHECK
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
SEEK ERROR
```

where zzz should be 287

One or more of the lightface message lines will appear depending on whether or not that kind of error occurs.

3. If an error of Write Sector Command occurs, the following is displayed:

```
*TEST FAILED--TEST STEP   zzz
WRITE SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY
```

where zzz should be 288 through 300
d should be A OR B

s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7

The error message lines printed above in lightface type will appear on the screen depending on whether or not this kind of error occurs. After the very first error, the operation will retry 10 times, and the following message will be displayed afterwards:

```
*TEST FAILED--TEST STEP   zzz
COMMAND RETRYING COUNT DOWN yy TIMES
WRITE SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY
```

where yy should be 1 through 9
zzz should be 288 through 300
d should be A OR B
s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7

One or more of the lightface message lines will appear on the screen depending on whether or not that kind of error occurs.

4. If an error of Read Sector Command occurs, the following is displayed:

```
*TEST FAILED--TEST STEP   zzz
READ SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
```

```
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY
```

where zzz should be 288 through 300
d should be A OR B
s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7

The error message lines printed above in lightface type will appear on the screen depending on whether or not this kind of error occurs. After the very first error, the operation will retry 10 times, and the following message will be displayed afterwards:

```
*TEST FAILED--TEST STEP   zzz
COMMAND RETRYING COUNT DOWN yy TIMES
READ SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY
```

where yy should be 1 through 9
zzz should be 276, 279, 282, 285
d should be A OR B
s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7

One or more of the lightface message lines will appear on the screen depending on the number of errors.

5. If an error of Bad Sector Data occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
READ SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
```

```
ADDRESS=aaaaH
FAILED AT BYTE NUMBER nnnH
EXPECTED DATA=eeH
DATA READ=xxH

where zzz should be 288 through 300
      d should be A OR B
      s should be 0 OR 1
      ttt should be 000 through 039
      rr should be 1 through 7
      aaaa should be 0001, 0002, 0004, 0008, 0010, 0020, 0040
                     0080, 0100, 0200, 0400, 0800, 4000
      nnn should be 000 through 200
      ee should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80
      xx should be 00 through FF
```

TITLE: FDC RANDOM PATTERN TEST

TARGET LOGIC: 3C, 3D, 1D, 2D, 4D, 2B.2C, 1C, 1A, 1B, 3B, 2A, 13B, 12B, 12A, 11B, 9A, 9B and disk driver logic.

DESCRIPTION: The FDC Random Pattern Test is functionally tested by using DMA data transfer, writing a random sector in a random track 512 random pattern bytes, reading the sector back, and comparing the Read Buffer and the Write Buffer. For each sort, there are 128 tries for each random track, random sector, and the random 512 data bytes in each sector. The following table indicates the drive, side, disk operation and data pattern being tested for the various diagnostic test steps:

TEST STEP	DRIVE	SIDE	DISK OPERATION	DATA PATTERN
301	A	0	SENSE DRIVE READY	NONE
302	A	0	RETRACK TO 0	NONE
303	A	0	SECTOR W/R/VERIFY	RANDOM
304	A	1	SENSE DRIVE READY	NONE
305	A	1	RETRACK TO 0	NONE
306	A	1	SECTOR W/R/VERIFY	RANDOM
307	B	0	SENSE DRIVE READY	NONE
308	B	0	RETRACK TO 0	NONE
309	B	0	SECTOR W/R/VERIFY	RANDOM
310	B	1	SENSE DRIVE READY	NONE
311	B	1	RETRACK TO 0	NONE
312	B	1	SECTOR W/R/VERIFY	RANDOM

ERROR MESSAGE:

1. If an error of Sense Drive Status Command error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
FDD NOT READY
```

Afterwards, the diagnostic will retry 10 times to get the operator's attention. In the event that the error is not real, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
COMMAND RETRYING COUNT DOWN yy TIMES
FDD NOT READY
```

where zzz should be 301, 304, 307, 310
yy should be 1 through 9

2. If an error of Recalibrate Command occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
FDD EQUIPMENT CHECK

ABNORMAL TERMINATION
INVALID COMMAND
```

FDD READY CHANGE
SEEK ERROR

where zzz should be 302, 305, 308, 311

One or more of the lightface message lines will appear on the screen depending on whether or not that kind of error occurs.

3. If an error of Write Sector Command occurs, the following is displayed:

***TEST FAILED--TEST STEP zzz**
WRITE SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY

where zzz should be 303, 306, 309, 312
d should be A OR B
s should be 0 OR 1
ttt should be 000 through 039
rr should be 1 through 7

The error message lines printed above in lightface type will appear on the screen depending on whether or not this kind of error occurs. After the very first error, the operation will retry 10 times, and the following message will be displayed afterwards:

***TEST FAILED--TEST STEP zzz**
COMMAND RETRYING COUNT DOWN yy TIMES
WRITE SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY

ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK

```
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY

where yy should be 1 through 9
      zzz should be 303, 306, 309, 312
      d should be A OR B
      s should be 0 OR 1
      ttt should be 000 through 039
      rr should be 1 through 7
```

One or more of the lightface message lines will appear on the screen depending on whether or not that kind of error occurs.

4. If an error of Read Sector Command occurs, the following is displayed:

```
*TEST FAILED--TEST STEP   zzz
READ SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY

where zzz should be 303, 306, 309, 312
      d should be A OR B
      s should be 0 OR 1
      ttt should be 000 through 039
      rr should be 1 through 7
```

The preceding error message lines that are printed in lightface type will appear on the screen depending on whether or not this kind of error occurs. After the very first error, the operation will retry 10 times, and the following message will be displayed afterwards:

```
*TEST FAILED--TEST STEP   zzz
```

```
COMMAND RETRYING COUNT DOWN yy TIMES
READ SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FDC BUSY IN READ/WRITE
FDD1 BUSY
FDD0 BUSY
FDD NOT READY
ABNORMAL TERMINATION
INVALID COMMAND
FDD READY CHANGE
END OF LAST TRACK
ID/DATA FIELD CRC ERROR
FDC OVERRUN
FDC DETECT NOT WRITABLE
MISSING ADDRESS MARK
DATA FIELD CRC ERROR
WRONG CYLINDER
BAD TRACK
FDD NOT READY
where yy should be 1 through 9
      zzz should be 276,279, 282, 285
      d should be A OR B
      s should be 0 OR 1
      ttt should be 000 through 039
      rr should be 1 through 7

      One or more of the lightface message lines will appear on the
      screen depending on the number of errors.
```

5. If an error of Bad Sector Data occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   zzz
READ SECTOR COMMAND
DRIVE d SIDE s TRACK ttt SECTOR rr
FAILED AT BYTE NUMBER nnnH
EXPECTED DATA=eeH
DATA READ=xxH
where zzz should be 303, 306, 309, 312
      d should be A OR B
      s should be 0 OR 1
      ttt should be 000 through 039
      rr should be 1 through 7
      aaaa should be 0001, 0002, 0004, 0008, 0010, 0020, 0040
                     0080, 0100, 0200, 0400, 0800, 4000
      nnn should be 000 through 200
      ee should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80
      xx should be 00 through FF
```

TITLE: 8253 COUNTER 0 TEST

TARGET LOGIC: 4B, 6D, 8B and °GATE' signal from clock/threshold board.

DESCRIPTION: The 8253 Counter 0 Test is functionally tested by using a programmable one shot mode and getting a 2 mhz °GATE' signal from clock threshold board. Then the counter 0 is verified by reading the counter 0 and comparing it to the expected count.

The following table indicates the 8253 counter 0 being tested for the diagnostic test step 313:

TEST STEP	8253 COUNTER	8253 MODE
313	COUNTER 0	MODE 1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP       313
8253 COUNTER 0 TEST
TERMINAL COUNT S/B ccccH
READ BACK COUNT WAS rrrrH

where cccc should be FDFA
      rrrr should be >FE00 or <FDF0
```

This section describes the subtests executed on the K105-D KEYBOARD /DISPLAY board, and the associated error reporting and methodology of programming.

The keyboard/display diagnostic is divided into 7 subtests, each described individually on the following pages.

Subtest 1 is a keyboard logic test. Subtests 2 through 6 are interrupt request lines (INTR3/ through INTR7/) tests. Subtest 7 is a dip switch 'S1' integrity test.

Subtests 2 through 6 not only test the 8259A interrupt controller logic for the data display board but also test 5 interrupts generated on the I/O option board.

> NOTE: The 'TARGET LOGIC' listed in each subtest description does not necessarily include all of the logic which could affect the operation of that subtest.

SUBTEST CATEGORIES

1. KEYBOARD TEST
2. INTR3/(FDC) TEST
3. INTR4/(8253 COUNTER 0) TEST
4. INTR5/(8251 #2) TEST
5. INTR6/(8251 #1) TEST
6. INTR7/(8291 GPIB) TEST

ERROR COUNT CATEGORIES

1. KEY CODE ERROR COUNT
2. STUCK KEY ERROR COUNT
3. INTR3/ ERROR COUNT
4. INTR4/ ERROR COUNT
5. INTR5/ ERROR COUNT
6. INTR6/ ERROR COUNT
7. INTR7/ ERROR COUNT
8. DIP SWITCH ERROR COUNT

TITLE: KEYBOARD TEST

TARGET LOGIC: 8E,14E,13E,10E and keyboard interface matrix

DESCRIPTION: The keyboard logic is functionally tested by pressing a specified key in the front panel, reading the corresponding I/O port from buffer (10E), and then verifying the key data to the expected data.

After key data has been verified, the stacked keys are tested by scanning the whole keyboard interface.

There are 48 keys in the front panel, the corresponding I/O port 1XH are arranged as follows:

a. X = 0 if key is located at column 1 in the front panel

b. X = 2 if key is located at column 2 in the front panel

c. X = 4 if key is located at column 3 in the front panel

d. X = 6 if key is located at column 4 in the front panel

e. X = 8 if key is located at column 5 in the front panel

f. X = A if key is located at column 6 in the front panel

h. X = C if key is located at column 7 in the front panel

i. X = E if key is located at column 8 in the front panel.

There are 6 key data read from the buffer (10E), they are arranged as follows:

a. The key data read = FEH if the key is located at row 1 in the front panel

b. The key data read = FDH if the key is located at row 2 in the front panel

c. The key data read = FBH if the key is located at row 3 in the front panel

d. The key data read = F7H if the key is located at row 4 in the front panel

e. The key data read = EFH if the key is located at row 5 in the front panel

f. The key data read = DFH if the key is located at row 6 in the front panel

The following information message will be displayed before each key is tested:

```
>TESTING KEY ?????????????
>KEY NOT PRESSED YET,PRESS IT!
```

where ????????????? could be 1 character,for example,"0" through "9","A" through "F", or up to 13 characters,for example,"TRACE CONTROL" in the domain of 48 defined keys.

"EDIT" and "STOP" are special keys where all interrupts are disabled whenever testing these two keys. Testing keys other than "EDIT" or "STOP" will have an interrupt enabled time for the diagnostic monitor to scan the whole keyboard and respond to special keys "EDIT" or "STOP".

The following table indicates the key under test and the category being tested for the various diagnostic test step:

TEST STEP	KEY TESTED	CATEGORY OF TEST
1	"NEXT"	KEY CODE MATCH
2	"NEXT"	STUCK KEY CHECK
3	"PREV"	KEY CODE MATCH
4	"PREV"	STUCK KEY CHECK
5	"FORMAT"	KEY CODE MATCH
6	"FORMAT"	STUCK KEY CHECK
7	"CLOCKS"	KEY CODE MATCH
8	"CLOCKS"	STUCK KEY CHECK
9	"TRACE CONTROL"	KEY CODE MATCH
10	"TRACE CONTROL"	STUCK KEY CHECK
11	"ARM MODE"	KEY CODE MATCH
12	"ARM MODE"	STUCK KEY CHECK
13	"UP ARROW"	KEY CODE MATCH
14	"UP ARROW"	STUCK KEY CHECK
15	"<--"	KEY CODE MATCH
16	"<--"	STUCK KEY CHECK
17	"DATA"	KEY CODE MATCH
18	"DATA"	STUCK KEY CHECK
19	"TIMING"	KEY CODE MATCH
20	"TIMING"	STUCK KEY CHECK
21	"GRAPH"	KEY CODE MATCH
22	"GRAPH"	STUCK KEY CHECK
23	"ANALYSIS"	KEY CODE MATCH
24	"ANALYSIS"	STUCK KEY CHECK
25	"-->"	KEY CODE MATCH
26	"-->"	STUCK KEY CHECK
27	"DOWN ARROW"	KEY CODE MATCH
28	"DOWN ARROW"	STUCK KEY CHECK
29	"A/B"	KEY CODE MATCH
30	"A/B"	STUCK KEY CHECK
31	"MAIN/HS"	KEY CODE MATCH
32	"MAIN/HS"	STUCK KEY CHECK
33	"SEARCH"	KEY CODE MATCH
34	"SEARCH"	STUCK KEY CHECK
35	"COMPARE"	KEY CODE MATCH
36	"COMPARE"	STUCK KEY CHECK
37	"CONTROL"	KEY CODE MATCH
38	"CONTROL"	STUCK KEY CHECK
39	"REF"	KEY CODE MATCH
40	"REF"	STUCK KEY CHECK
41	"C"	KEY CODE MATCH
42	"C"	STUCK KEY CHECK
43	"8"	KEY CODE MATCH
44	"8"	STUCK KEY CHECK
45	"4"	KEY CODE MATCH
46	"4"	STUCK KEY CHECK
47	"0"	KEY CODE MATCH
48	"0"	STUCK KEY CHECK

TEST STEP	KEY TESTED	CATEGORY OF TEST
49	"SHIFT"	KEY CODE MATCH

```
50          "SHIFT"         STUCK KEY CHECK
51          "HELP"          KEY CODE MATCH
52          "HELP"          STUCK KEY CHECK
53          "D"             KEY CODE MATCH
54          "D"             STUCK KEY CHECK
55          "9"             KEY CODE MATCH
56          "9"             STUCK KEY CHECK
57          "5"             KEY CODE MATCH
58          "5"             STUCK KEY CHECK
59          "1"             KEY CODE MATCH
60          "1"             STUCK KEY CHECK
61          "I/O"           KEY CODE MATCH
62          "I/O"           STUCK KEY CHECK
63          ""X""           KEY CODE MATCH
64          ""X""           STUCK KEY CHECK
65          "E"             KEY CODE MATCH
66          "E"             STUCK KEY CHECK
67          "A"             KEY CODE MATCH
68          "A"             STUCK KEY CHECK
69          "6"             KEY CODE MATCH
70          "6"             STUCK KEY CHECK
71          "2"             KEY CODE MATCH
72          "2"             STUCK KEY CHECK
73          "EDIT"          KEY CODE MATCH
74          "EDIT"          STUCK KEY CHECK
75          "INS"           KEY CODE MATCH
76          "INS"           STUCK KEY CHECK
77          "F"             KEY CODE MATCH
78          "F"             STUCK KEY CHECK
79          "B"             KEY CODE MATCH
80          "B"             STUCK KEY CHECK
81          "7"             KEY CODE MATCH
82          "7"             STUCK KEY CHECK
83          "3"             KEY CODE MATCH
84          "3"             STUCK KEY CHECK
85          "ARM"           KEY CODE MATCH
86          "ARM"           STUCK KEY CHECK
87          "STOP"          KEY CODE MATCH
88          "STOP"          STUCK KEY CHECK
89          "F1"            KEY CODE MATCH
90          "F1"            STUCK KEY CHECK
91          "F2"            KEY CODE MATCH
92          "F2"            STUCK KEY CHECK
93          "F3"            KEY CODE MATCH
94          "F3"            STUCK KEY CHECK
95          "F4"            KEY CODE MATCH
96          "F4"            STUCK KEY CHECK
```

ERROR MESSAGE:

1. If a key data error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP    ss
KEY DATA EXPECTED=eeH
KEY DATA READ =ddH
KEY DATA CODE READ="?????????????"

where ss should odd number 1 through 95
      ee should be FE,FD,FB,F7,EF,DF
      dd should be 00 through FF
      "?????????????"  should be any  key  in
      the domain of the 48 defined keys.
```

2. If a stacked key error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP    ss
STACKED KEY WAS "?????????????"

where ss should be even number 2 through 96
      "?????????????"  should be any  key  in
      the domain of the 48 defined keys.
```

TITLE: INTR3/TEST

TARGET LOGIC: 4E, 2E, 8E, 10E,8D, 9D, 10D and (8272 INT pin), 2D in I/O option board

DESCRIPTION: The INTR3/ interrupt logic is functionally tested by using the RECALIBRATE command of 8272 FDC chip to generate an interrupt and executing an interrupt service routine which sets a flag byte indicating the interrupt occurred.

Drive A and side 0 are used for FDC RECALIBRATE command.

The following table indicates the interrupt source and line for the diagnostic test step:

TEST STEP	INTERRUPT FROM	ON BOARD	INTERRUPT LINE
97	8272	I/O	INTR3/

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   97
INTR3/ NOT GENERATED
```

Keyboard/Display Board Subtest 3

TITLE: INTR4/ TEST

TARGET LOGIC: 4E, 2E, 8E, 10E, 8D, 9D, 10D and (8253 OUT0 pin), 3A in I/O option board

DESCRIPTION The INTR4/ interrupt logic is functionally tested by using the 8253 counter 0 under mode 0 to generate an interrupt INTR4/ and executing an interrupt service routine to set a flag byte indicating the interrupt occurred.

The following table indicates the interrupt source and line for the diagnostic test step:

TEST STEP	INTERRUPT FROM	ON BOARD	INTERRUPT LINE
98	8253 counter 0	I/O	INTR4/

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   98
INTR4/ NOT GENERATED
```

TITLE: INTR5/TEST

TARGET LOGIC: 4E, 2E, 8E, 10E, 8D,9D,10D and (USART #2 pin 15), 8A in I/O option board

DESCRIPTION: The INTR5/ interrupt logic is functionally tested by using the 8251A USART #2 TxRDY pin to generate an interrupt INTR5/ and executing an interrupt service routine to set a flag byte indicating the interrupt occurred.

Before doing this test, an RS232 wrap back connector must be installed.

The following table indicates the interrupt source and line for the diagnostic test step:

TEST STEP	INTERRUPT FROM	ON BOARD	INTERRUPT LINE
99	8251A USART #2	I/O	INTR5/

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED--TEST STEP   99
INTR5/ NOT GENERATED
```

TITLE: INTR6/TEST

TARGET LOGIC: 4E, 2E, 8E, 10E, 8D, 9D, 10D and (USART #1 pin 15), 8A in I/O option board

DESCRIPTION: The INTR6/ interrupt logic is functionally tested by using the 8251A USART #1 TxRDY pin to generate an interrupt INTR6/ and executing an interrupt service routine to set a flag byte indicating the interrupt occurred.

Before doing this test, an RS232 wrap back connector must be installed.

The following table indicates the interrupt source and line for the diagnostic test step:

TEST STEP	INTERRUPT FROM	ON BOARD	INTERRUPT LINE
100	8251A USART #1	I/O	INTR6/

ERROR MESSAGE:

If an error occurs, the following message is displayed:

*TEST FAILED--TEST STEP 100
INTR6/ NOT GENERATED

TITLE: INTR7/ TEST

TARGET LOGIC: 4E,2E,8E,10E, 8D,9D,10D and (17A INT pin), 13A, 9A in I/O option board

DESCRIPTION: The INTR7/ interrupt logic is functionally tested by using the 8291 GPIB INT pin 11 to generate an interrupt INTR7/ and executing an interrupt service routine to set a flag byte indicating the interrupt occurred.

The following table indicates the interrupt source and line for the diagnostic test step:

TEST STEP	INTERRUPT FROM	ON BOARD	INTERRUPT LINE
101	8291 GPIB	I/O	INTR7/

ERROR MESSAGE:

If an error occurs, the following message is displayed:

*TEST FAILED--TEST STEP 101
INTR7/ NOT GENERATED

SUBTEST 1 POWER SUPPLY AND FIXED THRESHOLDS TEST

SUBTEST 2 DAC TEST

SUBTEST 3 VARIABLE THRESHOLD STEERING TEST

SUBTEST 4 ECL THRESHOLD STEERING TEST

SUBTEST 5 TTL THRESHOLD STEERING TEST

SUBTEST 6 CLOCK TREE OUTPUT LINES TEST

SUBTEST 7 CLOCK TREE MUX SELECT TEST

SUBTEST 8 CLOCK TREE EDGE SELECT TEST

SUBTEST 9 INTERNAL CLOCK TEST

ADC CIRCUIT DESCRIPTION

CLOCK THRESHOLD PORT DESCRIPTIONS

TITLE: POWER SUPPLY AND FIXED THRESHOLDS TEST

TARGET LOGIC: 12B 11B 11C 10C 10D 10B 9B 9C 9D

PURPOSE: The purpose of this subtest is to check the power supply and fixed threshold (VARIABLE, ECL & TTL) voltages on the Clock Threshold board. This test will verify that the voltages and thresholds are within the specified tolerances defined in K105 System Specification.

DESCRIPTION: The P/S voltages and fixed thresholds are selected and tested in the following order:

TEST STEP	VOLTAGE/THRESHOLD	LOCATION	I/O PORT 21
001	AGND	Mux 1 12B-9	0FH
002	+15volts/2	Mux 1 12B-4	08H
003	-15volts/2	Mux 1 12B-5	09H
004	+5.0volts	Mux 1 12B-6	0AH
005	+6.2volts	Mux 1 12B-7	0BH
006	-5.2volts	Mux 1 12B-12	0CH
007	-6.2volts	Mux 1 12B-11	0DH
008	-5.12volts	Mux 1 12B-10	0EH
009	TTL(-1.4v)	Mux 3 11B-12	14H
010	ECL(+1.3v)	Mux 3 11B-11	15H
* 011	VAR/2(0.0v)	Mux 3 11B-10	16H

*** REFER TO THE ADC CIRCUIT DESCRIPTION ***
*** LOCATED IN THIS DOCUMENT FOR A MORE ***
*** DETAILED DESCRIPTION OF THE ADC CKT ***

The test first selects AGND (analog ground) on the CLOCK/THRESHOLD board. The ADC is then allowed to begin the conversion process. The ADC is then read, which is accomplished by reading port 28 (READ ADC) twice since the ADC requires 10 binary bits to encode the voltage data.

* Prior to testing the VAR Threshold a 20H is written to PORT 20 (DACWR) to set the VAR Threshold equal to 0.00 volts.

The first ADC data byte read contains the MSN (Most Significant Nibble) and LSN (Least Significant Nibble) hex data. The second byte contains the LSB (Least Significant Bits) which are located in bits BD6 and BD7. All other data bits in the second byte read are not used.

The data obtained in the two (2) reads of the ADC are used as an index to a table of voltage values. This is accomplished by multiplying the ADC data by 2 and using the result as an index pointer to the corresponding voltage value in the table. The voltage values in the table are read and the result is computed by the following formula:

$$VI = [\ V(MSN) + V(LSN) + V(LSB) - 2560\ ] \times 4 \qquad [mv]$$

The resulting value obtained is compared to an upper and lower tolerance value, and an error is reported if the ADC result is out of tolerance.

Due to the inherent error factor in the ADC circuit a CV (Compensation Value) must be computed prior to each voltage reading of the ADC. CV is determined by selecting AGND and reading the ADC and computing the result as shown in the formula as follows:

CV = Vr - 2560 [mv]x

where

Vr = V(MSN) + V(LSN) + V(LSB) [mv]

The CV computed is subtracted from the subsequent voltage reading.

NOTE: The reason for testing AGND first is that since all ADC readings are referenced to AGND, AGND must be determined to be within the specified tolerance allowed before any subsequent voltage readings of the ADC can be considered accurate. The diagnostic, however, does allow the operator to check other voltages even if AGND is out of tolerance but the error message returned will indicate that a CV value of 0.00 volts was used, therefore the ADC voltage read will not be correct.

ERROR MESSAGE:

```
        *TEST FAILED:        TEST STEP zzz
        ADC ERROR-TESTING '----------------------------'
        VOLTAGE EXPECTED     yy.yy V
        VOLTAGE READ         xx.xx V
        UPPER TOLERANCE      ww.ww V
        LOWER TOLERANCE      uu.uu V

        ADC DATA READ          1ST READ = ssH     2ND READ = vvH

**      AGND OUT OF TOLERANCE - COMP. VALUE = 0.00v
```

where

zzz	=	TEST STEP NUMBER
'-----'	=	VOLTAGE CKT BEING TESTED
yy.yy	=	ADC VOLTAGE EXPECTED
xx.xx	=	ADC VOLTAGE READ
ww.ww	=	UPPER VOLTAGE TOLERANCE
uu.uu	=	LOWER VOLTAGE TOLERANCE
ss	=	1ST ADC HEX DATA BYTE READ
vv	=	2ND ADC HEX DATA BYTE READ

** This message only appears when AGND or the CV value computed is determined to be out of tolerance.

Clock/Threshold Subtest 2

TITLE: DAC TEST

TARGET LOGIC: 9E 9D 9B 9C 11B 11C 10C 10D

PURPOSE: The purpose of this subtest is to test the DAC (at loc 9C) to ensure the correct voltage out for the data code written. The input data lines (BD0-BD7) are tested, in the process, for shorts and opens.

DESCRIPTION: This test is similar to subtest 1 in that it uses the ADC circuit to test the output of DAC (VAR/2). Refer to the ADC circuit description in this chapter for a more detailed description of the ADC test process.

The VAR/2 input (MUX 3-loc 11B pin 10) is selected by writing a 16H to PORT 21 (ADCSEL). A 80H is then written to PORT 20 (DACWR) to set the DAC output (VAR/2) to 0.00 volts. A walking '1' pattern is used to generate the DAC code written to the DAC. Each unique pattern written is a separate test and is tested as such. The data pattern is written to the DAC by writing the hex code to PORT 20 (DACWR). The data pattern is written as shown below:

TEST STEP	DAC DATA CODE	VAR THRESHOLD VOLTAGE
012	00H	-12.80 V
013	01H	-12.70 V
014	02H	-12.60 V
015	04H	-12.40 V
016	08H	-12.00 V
017	10H	-11.20 V
018	20H	- 9.60 V
019	40H	- 6.40 V
020	80H	+ 0.0 V

NOTE

SINCE THE ADC WILL MEASURE VAR/2
THESE LISTED VOLTAGES ARE TWICE IN
VALUE OF WHAT THE ADC WILL MEASURE

ERROR MESSAGE:

```
*TEST FAILED:        TEST STEP zzz
ADC ERROR-TESTING '----------------------------'
VOLTAGE EXPECTED     yy.yy V
VOLTAGE READ         xx.xx V
UPPER TOLERANCE      ww.ww V
LOWER TOLERANCE      uu.uu V

ADC DATA READ          1ST READ = ssH      2ND READ = vvH

**      AGND OUT OF TOLERANCE - COMP. VALUE = 0.00v
```

where

zzz	=	TEST STEP NUMBER
'-----'	=	VOLTAGE CKT BEING TESTED
yy.yy	=	ADC VOLTAGE EXPECTED
xx.xx	=	ADC VOLTAGE READ

ww.ww	=	UPPER VOLTAGE TOLERANCE
uu.uu	=	LOWER VOLTAGE TOLERANCE
ss	=	1ST ADC HEX DATA BYTE READ
vv	=	2ND ADC HEX DATA BYTE READ

** This message only appears when AGND or the CV value computed is determined to be out of tolerance.

TITLE: VARIABLE THRESHOLD STEERING TEST

TARGET LOGIC: 12E 11E 12D 11D 11F 12F 11G 12G 10E 10G 10F, 12H 11H 10H 11B 12C 11C 10C 10D

PURPOSE: The purpose of this subtest is to test the ability of the CLOCK/ THRESHOLD board to select the Variable Threshold and steer the threshold to all the probes.

DESCRIPTION: The Variable Threshold is set to 10.0 volts and the thresholds (TH-A thru TH-D1) are selected to the ECL Threshold inputs of their respective Analog Mux's (SWITCH's), which are at locations 12E, 11E, 12D, 11D, 11F, 12F, 11G, 12G, 10E, 10G, & 10F, respectively. This input selection causes the ECL Threshold to be routed to the threshold outputs of the Analog Switch's (TH-A thru TH-D1) and from there to the probes. The Analog Switch's input threshold selection is accomplished by writing the appropriate data code to I/O ports 22, 23, 26, & 27 (see the Clock/ Threshold I/O Port descriptions contained in this chapter).

The VAR/2 threshold is then routed to the appropriate threshold output under test (TH-A thru TH-D1) and then tested for the correct voltage level. The thresholds, TH-A thru TH-D1, are selected, to the VAR/2 threshold, and tested in the following order:

THRESHOLD	LOCATION
TH-A	12E
TH-B	11E
TH-C	12D
TH-D	11D
TH-E	11F
TH-F	12F
TH-G	11G
TH-H	12G
CTH-A	10G
CTH-B	10G
TH-D1	10E
TH-C1	10F

All threshold voltage levels are tested using the ADC circuit. This is accomplished by selecting the appropriate input to MUX 2 & 3 (loc 12C & 11B respectively), and then causing the ADC to convert the voltage. The ADC conversion process is the same as that described in subtest 1. The thresholds to be tested are selected as follows:

TEST STEP	VOLTAGE/THRESHOLD	LOCATION	I/O PORT 21
021	TH-A	Mux 2 12C-4	00H
022	TH-B	Mux 2 12C-5	01H
023	TH-C	Mux 2 12C-6	02H
024	TH-D	Mux 2 12C-7	03H
025	TH-E	Mux 2 12C-12	04H
026	TH-F	Mux 2 12C-11	05H
027	TH-G	Mux 2 12C-10	06H
028	TH-H	Mux 2 12C-9	07H
029	CTH-A	Mux 3 11B-4	10H
030	CTH-B	Mux 3 11B-5	11H
031	TH-D1	Mux 3 11B-6	12H
032	TH-C1	Mux 3 11B-7	13H

ERROR MESSAGE:

```
*TEST FAILED:        TEST STEP zzz
ADC ERROR-TESTING '----------------------------'
VOLTAGE EXPECTED     yy.yy V
VOLTAGE READ         xx.xx V
UPPER TOLERANCE      ww.ww V
LOWER TOLERANCE      uu.uu V

ADC DATA READ          1ST READ = ssH     2ND READ = vvH

**      AGND OUT OF TOLERANCE - COMP. VALUE = 0.00v
```

where

zzz	=	TEST STEP NUMBER
'-----'	=	VOLTAGE CKT BEING TESTED
yy.yy	=	ADC VOLTAGE EXPECTED
xx.xx	=	ADC VOLTAGE READ
ww.ww	=	UPPER VOLTAGE TOLERANCE
uu.uu	=	LOWER VOLTAGE TOLERANCE
ss	=	1ST ADC HEX DATA BYTE READ
vv	=	2ND ADC HEX DATA BYTE READ

** This message only appears when AGND or the CV value computed is determined to be out of tolerance.

TITLE: ECL THRESHOLD STEERING TEST

TARGET LOGIC: 12E 11E 12D 11D 11F 12F 11G 12G 10E 10G 10F, 12H 11H 10H 11B 12C 11C 10C 10D

PURPOSE: The purpose of this subtest is to test the ability of the CLOCK/THRESHOLD board to select the ECL Threshold and steer the threshold to all the probes.

DESCRIPTION: The Variable Threshold is set to 10.0 volts by writing a 0E4h to port 20 (DACWR). The thresholds (TH-A thru TH-D1) are selected to the VAR/2 Threshold inputs of their respective Analog Mux's (SWITCH's), which are at locations 12E, 11E, 12D, 11D, 11F, 12F, 11G, 12G, 10E, 10G, & 10F, respectively. This input selection causes the VAR/2 Threshold to be routed to the threshold outputs of the Analog Switch's (TH-A thru TH-D1) and from there to the probes. The Analog Switch's input threshold selection is accomplished by writing the appropriate data code to I/O ports 22, 23, 26, & 27 (see the Clock/Threshold I/O Port descriptions contained in this chapter).

The ECL threshold is then routed to the appropriate threshold output under test (TH-A thru TH-D1) and then tested for the correct voltage level. The thresholds, TH-A thru TH-D1, are selected, to the ECL threshold, and tested in the following order:

THRESHOLD	LOCATION
TH-A	12E
TH-B	11E
TH-C	12D
TH-D	11D
TH-E	11F
TH-F	12F
TH-G	11G
TH-H	12G
CTH-A	10G
CTH-B	10G
TH-D1	10E
TH-C1	10F

All threshold voltage levels are tested using the ADC circuit. This is accomplished by selecting the appropriate input to MUX 2 & 3 (loc 12C & 11B respectively), and then causing the ADC to convert the voltage.

The ADC conversion process is the same as that described in subtest 1. The thresholds to be tested are selected as follows:

TEST STEP	VOLTAGE/THRESHOLD	LOCATION	I/O PORT 21
033	TH-A	Mux 2 12C-4	00H
034	TH-B	Mux 2 12C-5	01H
035	TH-C	Mux 2 12C-6	02H
036	TH-D	Mux 2 12C-7	03H
037	TH-E	Mux 2 12C-12	04H
038	TH-F	Mux 2 12C-11	05H
039	TH-G	Mux 2 12C-10	06H
040	TH-H	Mux 2 12C-9	07H
041	CTH-A	Mux 3 11B-4	10H
042	CTH-B	Mux 3 11B-5	11H
043	TH-D1	Mux 3 11B-6	12H
044	TH-C1	Mux 3 11B-7	13H

ERROR MESSAGE:

```
*TEST FAILED:        TEST STEP zzz
ADC ERROR-TESTING '----------------------------'
VOLTAGE EXPECTED     yy.yy V
VOLTAGE READ         xx.xx V
UPPER TOLERANCE      ww.ww V
LOWER TOLERANCE      uu.uu V

ADC DATA READ          1ST READ = ssH      2ND READ = vvH

**       AGND OUT OF TOLERANCE - COMP. VALUE = 0.00v
```

where

zzz	=	TEST STEP NUMBER
'-----'	=	VOLTAGE CKT BEING TESTED
yy.yy	=	ADC VOLTAGE EXPECTED
xx.xx	=	ADC VOLTAGE READ
ww.ww	=	UPPER VOLTAGE TOLERANCE
uu.uu	=	LOWER VOLTAGE TOLERANCE
ss	=	1ST ADC HEX DATA BYTE READ
vv	=	2ND ADC HEX DATA BYTE READ

** This message only appears when AGND or the CV value computed is determined to be out of tolerance.

TITLE: TTL THRESHOLD STEERING TEST

TARGET LOGIC: 12E 11E 12D 11D 11F 12F 11G 12G 10E 10G 10F, 12H 11H 10H 11B 12C 11C 10C 10D

PURPOSE: The purpose of this subtest is to test the ability of the CLOCK/THRESHOLD board to select the TTL Threshold and steer the threshold to all the probes.

DESCRIPTION: The Variable Threshold is set to 10.0 volts by writing an 0E4h to port 20 (DACWR). The thresholds (TH-A thru TH-D1) are selected to the VAR/2 Threshold inputs of their respective Analog Mux's (SWITCH's), which are at locations 12E, 11E, 12D, 11D, 11F, 12F, 11G, 12G, 10E, 10G, & 10F, respectively. This input selection causes the VAR/2 Threshold to be routed to the threshold outputs of the Analog Switch's (TH-A thru TH-D1) and from there to the probes. The Analog Switch's input threshold selection is accomplished by writing the appropriate data code to I/O ports 22, 23, 26, & 27 (see the Clock/Threshold I/O Port descriptions contained in this chapter).

The TTL threshold is then routed to the appropriate threshold output under test (TH-A thru TH-D1) and then tested for the correct voltage level. The thresholds, TH-A thru TH-D1, are selected, to the TTL threshold, and tested in the following order:

THRESHOLD	LOCATION
TH-A	12E
TH-B	11E
TH-C	12D
TH-D	11D
TH-E	11F
TH-F	12F
TH-G	11G
TH-H	12G
CTH-A	10G
CTH-B	10G
TH-D1	10E
TH-C1	10F

All threshold voltage levels are tested using the ADC circuit. This is accomplished by selecting the appropriate input to MUX 2 & 3 (loc 12C & 11B respectively), and then causing the ADC to convert the voltage. The ADC conversion process is the same as that described in subtest 1.

The thresholds to be tested are selected as follows:

TEST STEP	VOLTAGE/THRESHOLD	LOCATION	I/O PORT 21
045	TH-A	Mux 2 12C-4	00H
046	TH-B	Mux 2 12C-5	01H
047	TH-C	Mux 2 12C-6	02H
048	TH-D	Mux 2 12C-7	03H
049	TH-E	Mux 2 12C-12	04H
050	TH-F	Mux 2 12C-11	05H
051	TH-G	Mux 2 12C-10	06H
052	TH-H	Mux 2 12C-9	07H
053	CTH-A	Mux 3 11B-4	10H
054	CTH-B	Mux 3 11B-5	11H
055	TH-D1	Mux 3 11B-6	12H
056	TH-C1	Mux 3 11B-7	13H

ERROR MESSAGE:

```
*TEST FAILED:        TEST STEP zzz
ADC ERROR-TESTING '----------------------------'
VOLTAGE EXPECTED     yy.yy V
VOLTAGE READ         xx.xx V
UPPER TOLERANCE      ww.ww V
LOWER TOLERANCE      uu.uu V

ADC DATA READ          1ST READ = ssH      2ND READ = vvH

**      AGND OUT OF TOLERANCE - COMP. VALUE = 0.00v
```

where

zzz	=	TEST STEP NUMBER
'-----'	=	VOLTAGE CKT BEING TESTED
yy.yy	=	ADC VOLTAGE EXPECTED
xx.xx	=	ADC VOLTAGE READ
ww.ww	=	UPPER VOLTAGE TOLERANCE
uu.uu	=	LOWER VOLTAGE TOLERANCE
ss	=	1ST ADC HEX DATA BYTE READ
vv	=	2ND ADC HEX DATA BYTE READ

** This message only appears when AGND or the CV value computed is determined to be out of tolerance.

TITLE: CLOCK TREE OUTPUT LINES TEST

TARGET LOGIC: 5D 5E 5F 5G 5J

PURPOSE: The purpose of this subtest is to test the clock output lines of the clock tree on the CLOCK/THRESHOLD board. The clock output lines are S0, S1, S2, S3, & MSTR.

DESCRIPTION: The thresholds (TH-A thru TH-D1) are set to the ECL threshold. This allows the leading edge inputs, to the clock tree, to be detected.

The clock tree MUX's (S0, S1, S2, S3, & MSTR) are then set to their respective leading edge inputs, ie: the S0 leading edge input to the S0 clock MUX is selected, the S1 leading edge input to the S1 clock MUX is selected.

All the leading edge inputs to the S0 clock tree are selected by writing 0AAH to Port 2F (S0CJ) and writing 55H to Port 2E (S0CK).

The clock status buffer (loc 5J) is then read, by reading port 20 (DACWR), and comparing the status byte read to the data expected. The S0, S1, S2, & S3 clock output lines are tested in this manner. The MASTER (MSTR) clock output line is tested by selecting the S0 leading edge input to the MSTR clock mux, and select-ing all S0 leading edge inputs to the clock tree. The clock status buffer is then read and compared to the data expected.

TEST STEP	CLOCK MUX OUTPUT	LOCATION
057	S0 CLK OUTPUT	5D pin 6
058	S1 CLK OUTPUT	5E pin 6
059	S2 CLK OUTPUT	5F pin 6
060	S3 CLK OUTPUT	5G pin 6
061	MSTR CLK OUTPUT	5C pin 6

ERROR MESSAGE:

```
*TEST FAILED--TEST STEP zzz
CLOCK SELECT TEST - '---------'
CLOCK BUFFER DATA EXPECTED = ww
CLOCK BUFFER DATA READ     = xx
```

where:

```
zzz     =     TEST STEP NUMBER
ww      =     DATA EXPECTED (IN HEX)
xx      =     DATA READ     (IN HEX)
```

TITLE: CLOCK TREE MUX SELECT TEST

TARGET LOGIC: 2D 4D 5D 1D 3D 5E 5F 5G 5C 5J

PURPOSE: The purpose of this subtest is to test the ability to select the clock tree MUX inputs correctly. This is accomplished by testing each individual MUX input separately, and then reading the clock status buffer for the result.

DESCRIPTION: The lowspeed clock threshold is set to the ECL level by writing the appropriate code (40h) to Port 26.

The S0 leading edge input to all the clock MUX's (loc 5D, 5E, 5F, 5G, & 5C) is then selected, by writing the appropriate code to ports 24 & 25. The clock status buffer, port 20 (loc 5J), is then read to insure that the level at the input to the MUX is correct when no clocks are enabled. If the MUX input level is not correct an error Msg is displayed.

Then all leading edge inputs to the S0 J section clock tree are enabled, by writing 0ffh to port 2F. This should cause the input level to the MUX's (S0 thru MSTR), to toggle. The status buffer is then read, by reading Port 20 (loc 5J), and the data read, is compared to the data expected.

The test is then repeated, testing the S1, S2, & S3 leading edge inputs to all the clock MUX's, as described in the preceding paragraph.

To test the trailing edge inputs to all the clock MUX's, the lowspeed clock threshold is set to the TTL level by writing the appropriate code (00h) to Port 26. By selecting the appropriate trailing edge inputs to the clock MUX's, the S0 thru MSTR clock MUX inputs are tested repeating the test as outlined above.

** NOTE **

LE = LEADING EDGE
TE = TRAILING EDGE

TEST STEP	CLK MUX INPUT LINES	LOCATION
062	S0 CLK (LE) MUX INPUT	5D pin 3
	S0 "	5E pin 3
	S0 "	5F pin 3
	S0 "	5G pin 3
	S0 "	5C pin 3
063	S1 CLK (LE) MUX INPUT	5D pin 1
	S1 "	5E pin 1
	S1 "	5F pin 1
	S1 "	5G pin 1
	S1 "	5C pin 1
064	S2 CLK (LE) MUX INPUT	5D pin 14
	S2 "	5E pin 14

	S2 "	5F pin 14
	S2 "	5G pin 14
	S2 "	5C pin 14
065	S3 CLK (LE) MUX INPUT	5D pin 12
	S3 "	5E pin 12
	S3 "	5F pin 12
	S3 "	5G pin 12
	S3 "	5C pin 12
066	S0 CLK (TE) MUX INPUT	5D pin 4
	S0 "	5E pin 4
	S0 "	5F pin 4
	S0 "	5G pin 4
	S0 "	5C pin 4
067	S1 CLK (TE) MUX INPUT	5D pin 2
	S1 "	5E pin 2
	S1 "	5F pin 2
	S1 "	5G pin 2
	S1 "	5C pin 2
068	S2 CLK (TE) MUX INPUT	5D pin 15
	S2 "	5E pin 15
	S2 "	5F pin 15
	S2 "	5G pin 15
	S2 "	5C pin 15
069	S3 CLK (TE) MUX INPUT	5D pin 13
	S3 "	5E pin 13
	S3 "	5F pin 13
	S3 "	5G pin 13
	S3 "	5C pin 13

ERROR MESSAGE:

```
*TEST FAILED--TEST STEP zzz
CLOCK SELECT TEST - '---------'
CLOCK BUFFER DATA EXPECTED = ww
CLOCK BUFFER DATA READ     = xx
```

where:

zzz	=	TEST STEP NUMBER
'--'	=	MUX INPUT LINE UNDER TEST
ww	=	DATA EXPECTED (IN HEX)
xx	=	DATA READ (IN HEX)

Clock/Threshold Subtest 8

TITLE: BLOCK TREE EDGE SELECT TEST

TARGET LOGIC: 1J 2J 3J 4J 1H 2H 3H 4H 2D 4D 5D 1G 2G 3G 4G 1D 3D, 5E 1F 2F 3F 4F 5F 1E 2E 3E 4E 5G 5C

PURPOSE: The purpose of this subtest is to test all the individual edge inputs to the clock tree.

DESCRIPTION: The appropriate lowspeed clock threshold (ECL or TTL) is selected for the clock edge under test. All MUX's are selected to the appropriate input for the clock edge under test. The clock edge to be tested is enabled. The status buffer at loc 5J is then read and if the data read is not correct an error is reported. The lowspeed clock threshold is then changed to toggle the clock edge under test. The status buffer is read again and if the data read is not correct an error is reported.

The trailing edge inputs are tested first, then the leading edge inputs to the S0, S1, S2, S3, & MSTR clock MUX's respectively. Please see subtest 7 and the I/O port description, contained in this chapter, for a more detailed description of this process.

** NOTE **
THIS TEST IS A STATIC TEST
AND A LOGIC HIGH IS EXPECTED
AT THE INPUT POINT OF ORIGIN

TEST STEP	PROBE THRESHOLD	CLOCK EDGE	LOCATION
070	ECL	S0 - CJA (TE)	3H pin 6
071	ECL	S0 - CJB (TE)	3H pin 11
072	ECL	S0 - CJC (TE)	4H pin 9
073	ECL	S0 - CJD (TE)	4H pin 11
074	TTL	S0 - CKA (TE)	1H pin 9
075	TTL	S0 - CKB (TE)	1H pin 11
076	TTL	S0 - CKC (TE)	2H pin 6
077	TTL	S0 - CKD (TE)	2H pin 11
078	ECL	S1 - CJA (TE)	3G pin 6
079	ECL	S1 - CJB (TE)	3G pin 11
080	ECL	S1 - CJC (TE)	4G pin 9
081	ECL	S1 - CJD (TE)	4G pin 11
082	TTL	S1 - CKA (TE)	1G pin 9
083	TTL	S1 - CKB (TE)	1G pin 11
084	TTL	S1 - CKC (TE)	2G pin 6
085	TTL	S1 - CKD (TE)	2G pin 11
086	ECL	S2 - CJA (TE)	3F pin 6
087	ECL	S2 - CJB (TE)	3F pin 11
088	ECL	S2 - CJC (TE)	4F pin 9
089	ECL	S2 - CJD (TE)	4F pin 11
090	TTL	S2 - CKA (TE)	1F pin 9
091	TTL	S2 - CKB (TE)	1F pin 11

092	TTL	S2 - CKC (TE)	2F pin 6
093	TTL	S2 - CKD (TE)	2F pin 11
094	ECL	S3 - CJA (TE)	3E pin 6
095	ECL	S3 - CJB (TE)	3E pin 11
096	ECL	S3 - CJC (TE)	4E pin 9
097	ECL	S3 - CJD (TE)	4E pin 11
098	TTL	S3 - CKA (TE)	1E pin 9
099	TTL	S3 - CKB (TE)	1E pin 11
100	TTL	S3 - CKC (TE)	2E pin 6
101	TTL	S3 - CKD (TE)	2E pin 11
102	TTL	S0 - CJA (LE)	3H pin 9
103	TTL	S0 - CJB (LE)	3H pin 3
104	TTL	S0 - CJC (LE)	4H pin 6
105	TTL	S0 - CJD (LE)	4H pin 3
106	ECL	S0 - CKA (LE)	1H pin 6
107	ECL	S0 - CKB (LE)	1H pin 3
108	ECL	S0 - CKC (LE)	2H pin 9
109	ECL	S0 - CKD (LE)	2H pin 3
110	TTL	S1 - CJA (LE)	3G pin 9
111	TTL	S1 - CJB (LE)	3G pin 3
112	TTL	S1 - CJC (LE)	4G pin 6
113	TTL	S1 - CJD (LE)	4G pin 3
114	ECL	S1 - CKA (LE)	1G pin 6
115	ECL	S1 - CKB (LE)	1G pin 3
116	ECL	S1 - CKC (LE)	2G pin 9
117	ECL	S1 - CKD (LE)	2G pin 3
118	TTL	S2 - CJA (LE)	3F pin 9
119	TTL	S2 - CJB (LE)	3F pin 3
120	TTL	S2 - CJC (LE)	4F pin 6
121	TTL	S2 - CJD (LE)	4F pin 3
122	ECL	S2 - CKA (LE)	1F pin 6
123	ECL	S2 - CKB (LE)	1F pin 3
124	ECL	S2 - CKC (LE)	2F pin 9
125	ECL	S2 - CKD (LE)	2F pin 3
126	TTL	S3 - CJA (LE)	3E pin 9
127	TTL	S3 - CJB (LE)	3E pin 3
128	TTL	S3 - CJC (LE)	4E pin 6
129	TTL	S3 - CJD (LE)	4E pin 3
130	ECL	S3 - CKA (LE)	1E pin 6
131	ECL	S3 - CKB (LE)	1E pin 3
132	ECL	S3 - CKC (LE)	2E pin 9
133	ECL	S3 - CKD (LE)	2E pin 3

ERROR MESSAGE:

```
*TEST FAILED--TEST STEP zzz
CLOCK SELECT TEST - '---------'
CLOCK BUFFER DATA EXPECTED = ww
CLOCK BUFFER DATA READ     = xx
```

where:

```
zzz      =       TEST STEP NUMBER
'--'     =       CLOCK EDGE UNDER TEST
ww       =       DATA EXPECTED (IN HEX)
xx       =       DATA READ     (IN HEX)
```

TITLE: INTERNAL CLOCK TEST

TARGET LOGIC: 1B 2B 1C 3B 3A 4A 5A 6A 7A 3C 2A 7B 7C 6B 6C 4B 5B 4C 5B

PURPOSE: The purpose of this subtest is to test the generation and routing of the low speed clocks and a frequency check of the 100 Mhz clock.

DESCRIPTION: A functional trace control board and I/O board must be present in the tested system before this subtest can be run. The trace control board presents, in the system, is checked by writing a 28h to port E0h and then reading port E0h. If a FFh is read from port E0h then the trace control board is determined to be not active and the test is aborted. An informational message to that effect is displayed.

The first test step (134) is to insure that counter #0 on the I/O board (loc 4B) is working correctly. This is accomplished by disabling the GLD signal from the trace control board, by writing an 80h to port E0H, and then, with no internal clock selected, read counter #0. If the count read from the counter has not been decremented, continue, otherwise report an error and abort the subtest. Then the counter is retested with an internal clock selected. If the count, read from the counter, otherwise report an error and abort the subtest.

Test steps 135 thru 146 test the ability to select and route the various internal clocks. The low speed clock circuit (LSCK-loc 5b pin 6) is tested first. The high speed clock circuit output is set to divide by one by writing a 40h to port 21h which also sets the CKTST signal (loc 5b pin 10) low enabling the selected clock to be routed to counter #0 on the I/O board. Then the low speed clock, to be tested, is selected by writing the appropriate code to I/O port 26. Counter #0 on the I/O board is initialized to mode 0 by writing a 30h to port 63h. The initial count (FFFFh) is written to the counter #0 which causes the counter to start. For every rising clock edge the counter decrements the count by one until the counter reaches 0000h. A time delay allows enough time for the counter to be decremented to 0 if the clock signal is present at the counter on the I/O board. After the time delay the count in the counter is read and if it is something other than zero an error is reported. After the low speed circuit is tested the high speed circuit (HSCK loc 5b pin 12) is tested in the same manner. The high speed clocks are selected by writing the appropriate code to port 27.

The low speed and high speed internal clocks are tested in the following order:

TEST STEP	INTERNAL CLOCK	LOCATION	I/O PORT
135	LS 10Mhz	loc 7c pin 2	32H to port 26
136	LS 1Mhz	loc 7c pin 1	2BH to port 26
137	LS 100Khz	loc 7c pin 15	1CH to port 26
138	LS 10Khz	loc 7c pin 14	1DH to port 26
139	LS 1Khz	loc 7c pin 13	1EH to port 26
140	LS 100 hz	loc 7c pin 12	1FH to port 26
141	HS 10Mhz	loc 7b pin 2	40H to port 27

142	HS 1Mhz	loc 7b pin 1	60H to port 27
143	HS 100Khz	loc 7b pin 15	80H to port 27
144	HS 10Khz	loc 7b pin 14	A0H to port 27
145	HS 1Khz	loc 7b pin 13	C0H to port 27
146	HS 100 hz	loc 7b pin 12	E0H to port 27

ERROR MESSAGE:

```
*TEST FAILED--TEST STEP zzz
INT CLK SELECT TEST - TESTING xxxxxxxxxxxxxxx
NO CLK OR INCORRECT CLOCK DETECTED
```

where

```
zzz  =   TEST STEP NUMBER
xxx  =   INT CLK BEING TESTED
```

Test step 147 is a test of the 100MHz frequency +- 1 %. This test is accomplished by using counter #0 in MODE 1 and the INT 4 line on the I/O board. First the current INT4 vector is saved by reading memory location 0090h and storing the value read. Memory location 0090 is then loaded with a pointer to the interrupt service routine for this test. The interrupt mask register is read and the data read is stored .

The CKTST SIGNAL is disabled by writing a C0h to port 21h. The 100Mhz int. clock is selected by writing a 2Fh to port 26h. Mode 1 is set in the counter by writing a 32h to port 63h. The count is then loaded into the counter by writing port 60h twice.

The count used will allow the counter to issue a INT4 when the counter reaches its terminal count indicating that the 100MHz frequency is below 101MHz. If no interrupt 4 was detected, an error message is displayed and the test is over. If an interrupt 4 was detected, the test is repeated with the count in the counter set for no interrupt 4 to occur indicating that the 100MHz frequency was above 99 MHz. If an interrupt 4 did occur the 100MHz is less than 99MHz and an error is reported.

ERROR MESSAGE:

```
*TEST FAILED--TEST STEP zzz
100 MHZ CLOCK FREQUENCY TEST
THE 100 MHZ APPEARS TO BE FAST
```

where

```
zzz  =   TEST STEP NUMBER
```

ERROR MESSAGE:

```
*TEST FAILED--TEST STEP zzz
100 MHZ CLOCK FREQUENCY TEST
THE 100 MHZ APPEARS TO BE SLOW
```

where

zzz = TEST STEP NUMBER

THE ADC CONVERSION PROCESS:

The successive approximation conversion process is started by reading port 20. Upon completion of a software time delay, the 10 bits can be read at port 28H by means of two reads, first the full byte and then the two least significant bits.

The voltage read (Vo) from the ADC is related to the input voltage (Vi) of the ADC circuitry by the following equation:

Vo=2560+Vi/4 [mV] (1)

To calculate the measured voltage, we rearrange equation (1):

Vi=(Vo-2560)*4 [mV] (2)

The ten bit code of the ADC can be obtained by reading the port S3CQ ('28H') twice and the following byte sequence is defined:

Byte order	Data bits of code								
	D07	D06	D05	D04	D03	D02	D01	D00	
	-- bits 9 through bits 2 of ADC code--								; first read
	bit1, bit0,0		0	0	0	0	0		; second read

For the purpose of the further discussion, we define the terms:

First reading:

D07	D06	D05	D04	
x	x	x	x	;Most Significant Nibble (MSN)

D03	D02	D01	D00	
X	X	X	X	;Least Signif. Nibble (LSN)

Second reading:

D07	D06	
X	X	;Least significant Bits (LSB)

Assuming an ideal ADC linearity and zero offset value, we can calculate the input voltage of the ADC by using the above mentioned groups as fractional binary values to determine the center values of the input resolution. With an ideal reference voltage adjustment of 2560 mV (Vref/2 input of ADC chip) the following table can be used to calculate the input voltage of the ADC (Vr) by using the formula:

Vr=V(MSN)+V(LSN)+V(LSB) [mV] (3)

Formula (3) substituted in formula (2) will give us a direct value of the Voltage (in mV) measured at the output of the analog multiplexers (MUX1-MUX3).

Vi=(V(MSN)+V(LSN)+V(LSB)-2560)*4 [mV] (4)

Note that an resistive translation circuit (Rp16) is used to generate the relationship of formula (1). The implementation of this table is necessary and the nibbles can be used as pointers to access these fractional values.

Hex:	Binary:	V(MSN):	V(LSN):	V(LSB): [mV]
0	(0 0)0 0	0000	0000	0000
1	(0 0)0 1	0320	0020	0005
2	(0 0)1 0	0640	0040	0010
3	(0 0)1 1	0960	0060	0015
4	0 1 0 0	1280	0080	-----
5	0 1 0 1	1600	0100	-----
6	0 1 1 0	1920	0120	-----
7	0 1 1 1	2240	0140	-----
8	1 0 0 0	2560	0160	-----
9	1 0 0 1	2880	0180	-----
A	1 0 1 0	3200	0200	-----
B	1 0 1 1	3520	0220	-----
C	1 1 0 0	3840	0240	-----
D	1 1 0 1	4160	0260	-----
E	1 1 1 0	4480	0280	-----
F	1 1 1 1	4800	0300	-----

ADC ADJUSTMENT:

The following is a brief discussion of the ADC adjustment problems that will have to be considered when writing the manufacturing test procedure for the clock/threshold board.

Reference Accuracy Requirements:

Since this ADC is used in an absolute conversion application, the initial value and the stability of the reference voltage (Vref/2) are important accuracy factors during the A/D conversion. For Vref/2 voltage of 2.56 V nominal value, an initial error of 2.5 mV will cause conversion errors of 1 LSB due to the gain of 2 of the Vref/2 input.

The magnitude of the reference voltage requires initial adjustment, since the error would directly appear as full-scale errors in the A/D conversion process. The ADC is configured to have the nominal span (no reduced or dynamic analog input voltage range) so that a zero error adjustment does not have to be done.

For initial adjustment of the ADC, a full-scale adjustment has to be done to compensate for the offset caused by the unequal biased inputs of the internal comparator circuit. This is done by injecting an external DC signal level which is one and a half LSB equivalent of the analog full-scale voltage less than it.

For this particular configuration the full scale voltage is 5.12 V, which will be reflected in a resolution of 5 mV so that we have to inject an accurate and low noise signal level of 5.1125 V (5.12-0.0075). We then observe the from the diagnostic software displayed and interpreted voltage and adjust the

reference voltage Vref/2 until we see the voltage just changing from 10.22V to 10.24 V. Note that the voltage displayed is not the voltage measured directly at the ADC input, since in normal operation we are only interested in the unscaled values.

This completes the adjustment procedure.

COMPUTING THE COMPENSATION VALUE:

In addition to the above described initial adjustment during the operation of the K105, we have to compensate for all temperature and non-linearity related error of the analog circuitry involved when making an ADC reading. This error should be determined, whenever the last reading was more than two minutes ago.

To calculate the compensation value (CV) we select and measure the analog ground, subtract the offset of the conversion circuitry (RP16). This is done by reading the ADC and subtracting 2560 mV from the value read. We call the resulting positive or negative value the 'compensation value;' it has to be added to each successive voltage read after adjusting for the scaling factor.

CV=Vr-2560 mV ;for Analog Ground selected (AGND) (5)

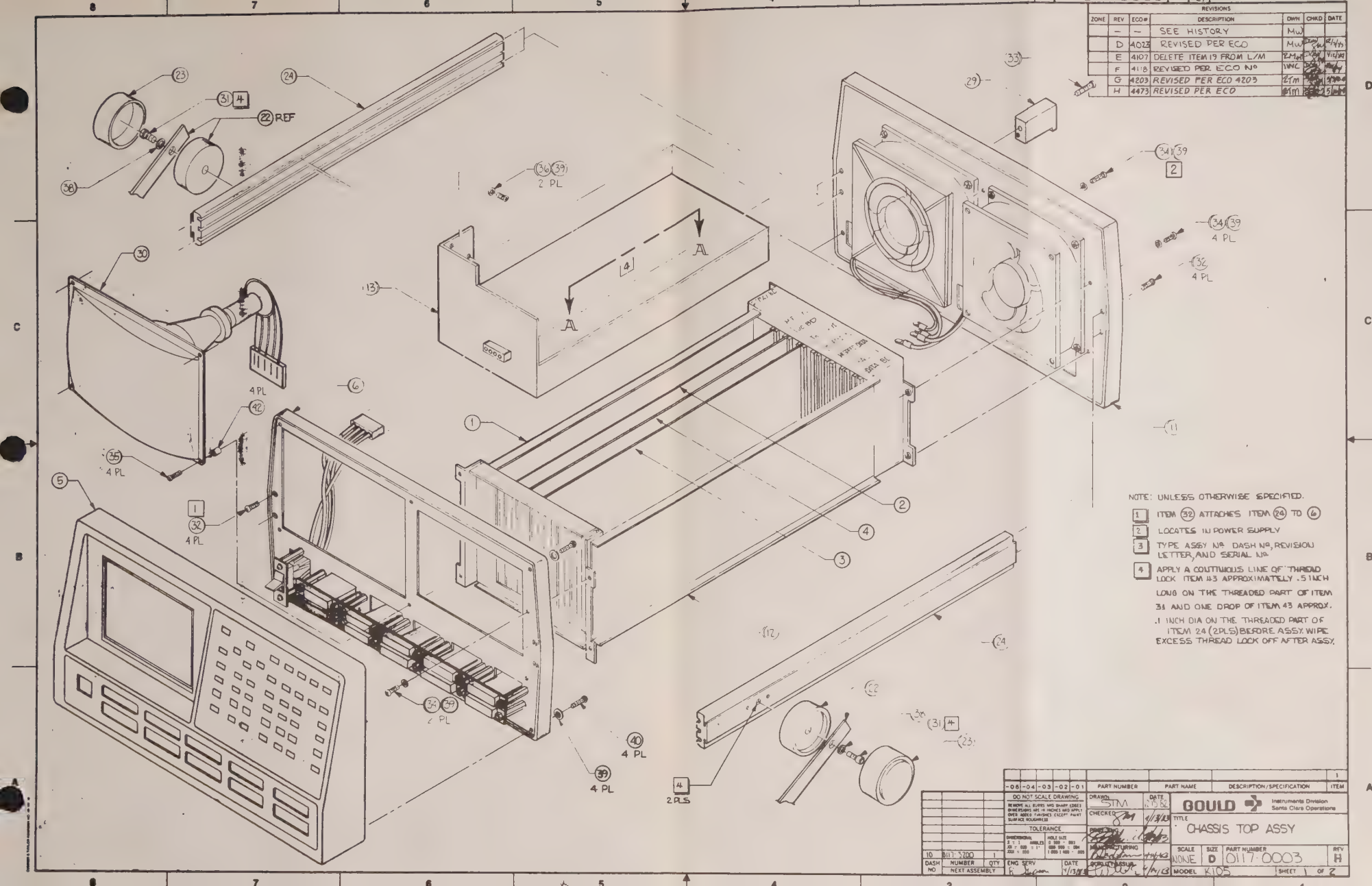
The tests specified will measure all fixed internal voltages, including the variable threshold voltage, which is set to 0.0V for this purpose. The measured values are compared with an upper and lower tolerance stored in a table. These values won't be available until the K105 is completely characterized.

DACWR: (PORT 20)

This byte is used to determine what the variable threshold should be.

BYTE CONTENT IN HEX	THRESHOLD AT PROBES
00	-12.8V
1C	-10.0V
80	0.00V
B2	5.00V
E4	10.00V
FF	12.70V

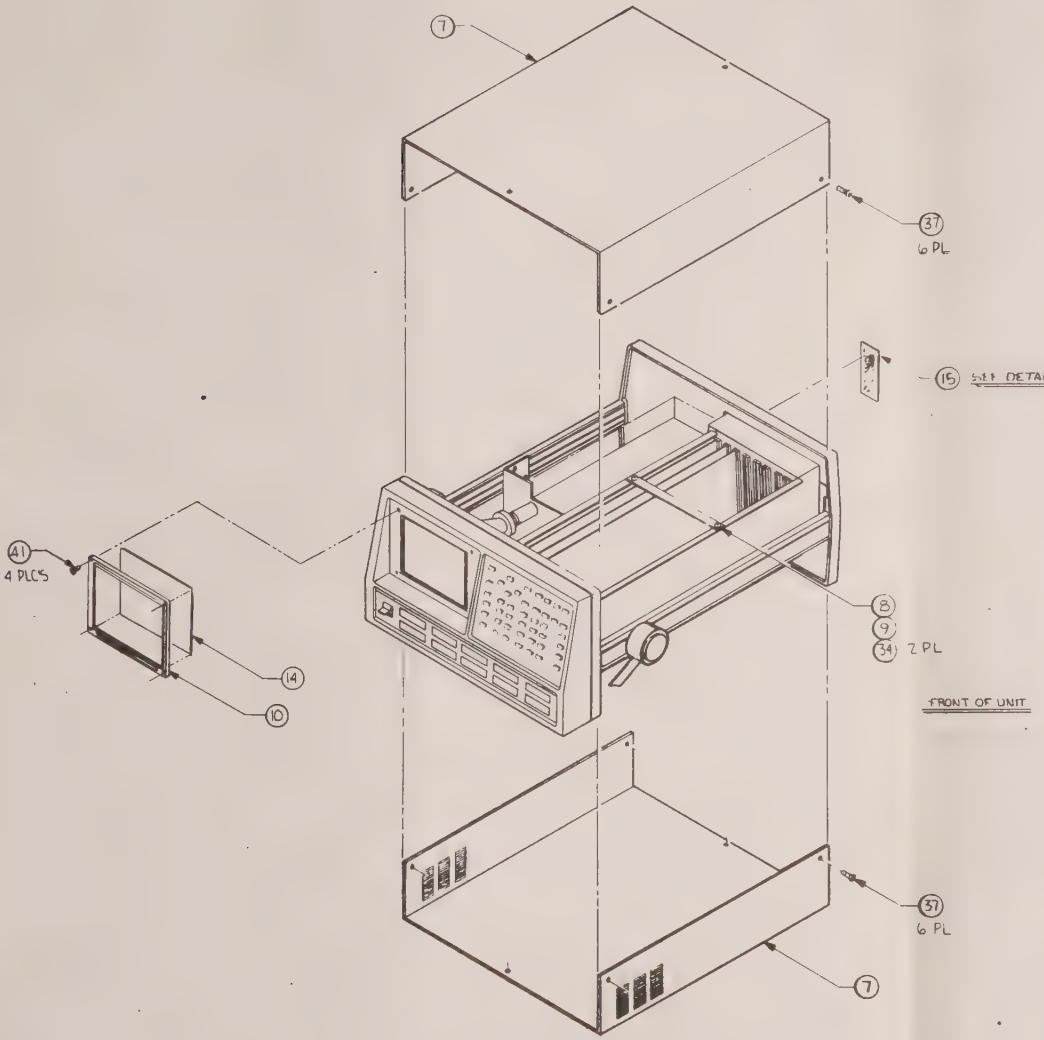
An increment/decrement to the byte content increases/decreases the threshold level by 100mV.

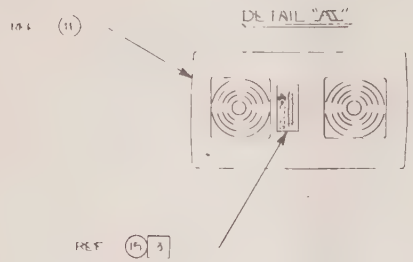


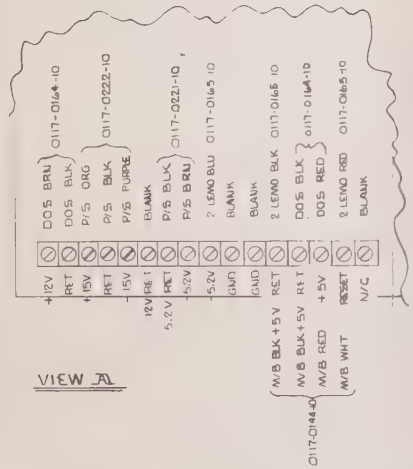
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
— | — | SEE HISTORY | MW
D | 4023 | REVISED PER ECO | MW
E | 4107 | DELETE ITEM 19 FROM L/M | RMW
F | 4118 | REVISED PER ECO No | WC
G | 4203 | REVISED PER ECO 4203 | RTM
H | 4473 | REVISED PER ECO | RTM
NOTE: UNLESS OTHERWISE SPECIFIED.
1 ITEM 32 ATTACHES ITEM 24 TO 6
2 LOCATES IN POWER SUPPLY
3 TYPE ASSY No DASH No, REVISION LETTER, AND SERIAL No
4 APPLY A CONTINUOUS LINE OF THREAD LOCK ITEM 43 APPROXIMATELY .5 INCH LONG ON THE THREADED PART OF ITEM 31 AND ONE DROP OF ITEM 43 APPROX. .1 INCH DIA ON THE THREADED PART OF ITEM 24 (2PLS) BEFORE ASSY. WIPE EXCESS THREAD LOCK OFF AFTER ASSY.
22 REF
2 PL
4 PL
2 PLS
DO NOT SCALE DRAWING
TOLERANCE
DRAWN STM
CHECKED
GOULD Instruments Division Santa Clara Operations
TITLE CHASSIS TOP ASSY
SCALE NONE
SIZE D
PART NUMBER 0117-0003
REV H
MODEL K105
SHEET 1 OF 2
10 | 0117-5700 | 1
DASH NO | NUMBER | QTY
NEXT ASSEMBLY
ENG SERV
DATE 4/13/83

0117-0003 [21]

REVISIONS						
ZONE	REV	ECO #	DESCRIPTION	DRWN	CHKD	DATE
			SEE SH. 1			







VIEW A

ITEM	PART NUMBER	PART NAME	DESCRIPTION / SPECIFICATION
-08			
-04			
-03			
-02			
-01			
1			

DO NOT SCALE DRAWING

TOLERANCE

DRAWN	DATE
STM	10/15/82
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR.	

GOULD Instruments Division Santa Clara Operations

TITLE: CHASSIS TOP ASSY

DASH NO.	NUMBER	QTY	ENG. REV.	DATE
10	0117-3200	1		

NEXT ASSEMBLY

SCALE	SIZE	PART NUMBER	REV
	D	0117-0003	H

MODEL K105 SHEET 2 OF 2

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	0114-2010-30	DATA DISPLAY SUB. ASSY		
2									1	0114-0185-70	SUB-ASSY MPU		
3									1	0117-0055-10	THRESHOLD / CLK PWA		
4									1	0117-0075-10	I/O BD ASSY		
5									1	0117-0008-10	FRONT BEZEL ASSY		
6									1	0117-0005-10	ASSY, FRONT CASTING		
7									2	0117-0142-20	COVER TOP + BOTTOM		
8									1	0117-0113-10	CARD RETAINER		
9									1	0117-0114-10	SUPPORT, CARD RETAINER		
10									1	0120-0019-40	CRT FILTER RETAINER		
11									1	0117-0006-10	REAR CASTING ASSY		
12									1	0117-0010-10	CARD CAGE ASSY		
13									1	9000-0137-01	ASSY POWER SUPPLY		
14									1	0120-0070-10	CRT FILTER		
15									1	#3030040	LABEL, MODEL		
16													
17													
18													
19													
20													
21													
22									1	0111-0016-10	HANDLE ASSY		
23									2	0111-0059-10	KNOB, BAIL		
24									2	0285-0117-30	EXTRUSION, SIDE RAIL GRAY		
25													
26													
27													

REV	DESCRIPTION	DATE	DWN	CKD
—	SEE HISTORY	—	—	—
F	REVISED PER ECO 4118	2/5/84	TWC	
G	REV'D PER ECO 4203	5/9/84	RTM	
H	REV'D PER ECO 4473	5/16/84	RTM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117-3200	1

		DATE
DWN	STM	8/24/83
CHK		9/13/83
ENGR		11/1/83
MFG		4-14-83
Q.A.		

LIST OF MATERIAL

CHASSIS ASSY

GOULD biomation

B | 0117-0003 | REV H

MODEL K105 | SHEET 1 OF 2

KLINGLER K-VEL H10

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
28													
29									1	0950-0099-10	FOOT REAR		
30									1	0117-0123-10	CRT ASSY		
31									2	7000 0376-10	SCR HD CAP	1/4-20 X 3/4 LG	
32									8	7000-0328-10	SCR PH H	THD ROLLING SCREW #8 x 5/8 LG	
33									1	7011-0832-60	SCR PAN HD	#8-32 X 1 3/8 LG.	
34									9	7011-0632-16	PAN HD SCR	6-32 x 1/2 LG	
35									4	7011-0632-20	PAN HD SCR	6-32 x 5/8 LG	
36									2	7011-0632-10	PAN HD SCR	6-32 x 5/16 LG	
37									12	7000-0606-10	SCR FLAT HD TYPE 'B'	#6 X .50 LG	
38									2	7085-0004-00	WASHER INT TOOTH STAR	1/4	
39									13	7085-0006-00	WASHER INT TOOTH STAR	#6	
40									4	7011-0000-12	SCREW, PH	#0-32 x 3/8 LG.	
41									4	7021-5440-12	SCREW FLAT HEAD	#4-40 X 3/8 LG. BLACK OXIDE	
42									4	7000-0320-10	SPACER RND	.140 I.D. x .25 O.D x .125 LG	
43									A/R	8200-0032-10	ADHESIVE THD LOK #262		

NOTES

LIST OF MATERIAL

CHASSIS TOP ASSY

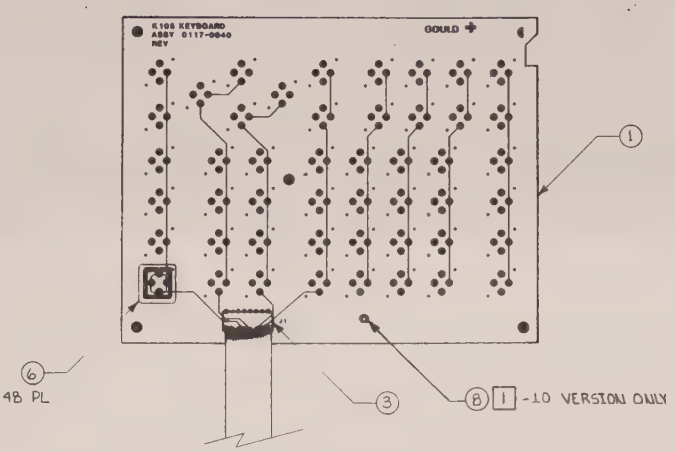
GOULD biomation

B | 0117-0003 | REV H

MODEL K105 | SHEET 2 OF 2

KLINGLER K-VEL H10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 316	SPN		2/3/83
	51	3695	REV'D PER ECO #	MW	DLW	4/6/83
	52	3739	REV'D PER ECO #	MW	DLW	5/3/83
	A	3957	PROD REL PER ECO	SWS	DLW	7/6/83
	B	4220	PER ECO	KR	DLW SWS	1/17/84



1 FLAT SIDE (CATHODE) OF ITEM 8 GOES TO SQUARE PAD ON CIRCUIT BOARD, -10 VERSION ONLY.

NOTES: UNLESS OTHERWISE SPECIFIED

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± 1°; XXX = .010

HOLE SIZE: 0.599 .003; .600 .999 .004; 1.000 1.499 .005

DASH NO	NUMBER NEXT ASSEMBLY	QTY
-20	0120-0008	1
-10	0117-0008	1

ENG SERV: R. Sagan — DATE: 2/18/83

DRAWN: J.W. CARROLL — DATE: 6-8-82

CHECKED: R. Wood — 2/18/83

PROD ENG: [signature] — 2-18-83

MANUFACTURING: [signature] — 2-18-83

QUALITY ASSUR

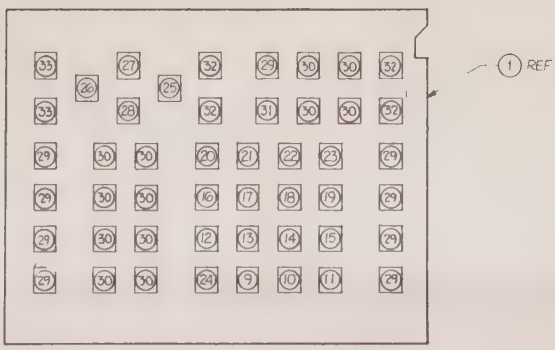
GOULD biomation

TITLE: ASSY — KEYBOARD

SCALE: 1:1 | SIZE: C | PART NUMBER: 0117-0040 | REV: B

CODE: K105 | SHEET 1 OF 2

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SH. 1	[illegible]		



-50	-40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± 1°; XXX = .010

HOLE SIZE: 0.599 .003; .600 .999 .004; 1.000 1.499 .005

DRAWN: [signature] — DATE: 12 7 82

CHECKED: R. Wood — 2-18-83

PROD ENG: [signature] — 2-18-83

MANUFACTURING: [signature] — 2-18-83

QUALITY ASSUR

GOULD biomation

TITLE: ASSEMBLY KEYBOARD

SCALE | SIZE: C | PART NUMBER: 0117-0040 | REV: B

CODE: K105 | SHEET 2 OF 2

DASH NO | NUMBER NEXT ASSEMBLY | QTY | ENG SERV: R. Sagan | DATE: 2/18/83

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1								1	1	0117-0042-10	K105 KEYBOARD PWB		
2													
3								1	1	0112-0204-10	CABLE ASSY KEY BD TO FRONT PANEL		L/M
4													
5													
6								48	48	6600-0118-10	SWITCH		
7													
8								—	1	6400-0039-10	L.E.D. RED	C.R.I.	
9								1	1	0112-0079-01	KEY TOP, WHITE	"1"	
10								1	1	-02		"2"	
11								1	1	-03		"3"	
12								1	1	-04		"4"	
13								1	1	-05		"5"	
14								1	1	-06		"6"	
15								1	1	-07		"7"	
16								1	1	-08		"8"	
17								1	1	-09		"9"	
18								1	1	-10		"A"	
19								1	1	-11		"B"	
20								1	1	-12		"C"	
21								1	1	-13		"D"	
22								1	1	-14		"E"	
23								1	1	-15		"F"	
24								1	1	0112-0079-16		"0"	
25								1	1	0112-0059-23	BLUE	"►"	
26								1	1	0112-0059-24		"◄"	
27								1	1	0112-0059-25	KEY TOP, BLUE	"▲"	

REV	DESCRIPTION	DATE	DWN	CKD
B	PER ECO 4220	1.17.83	Kaun	DGW
A	PROD REL PER 8957 C#	7/4/83	[illegible]	DGW
52	REV'D PER ECO # 3739	4/15/83	STM	DGW
51	REV'D PER ECO # 3695	4/5/83	MW	DGW
50	PILOT REL PER ERN 316	2.5.83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-20	0120-0008	1
-10	0117-0008	1

		DATE
DWN	J.W. CARROLL	6-4-82
CHK	R. Wood	2-15-83
ENGR	[signature]	2-18-83
MFG	[signature]	2-18-83
Q.A.		

LIST OF MATERIAL
ASSEMBLY
-KEYBOARD

GOULD biomation

B 0117-0040 REV B

MODEL K105 SHEET 1 OF 2

KLINGLER H-VEL H 10

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
28								1	1	0112-0059-26	KEY TOP BLUE	"▼"	
29								9	9	-0049-10	BLUE PLAIN		
30								12	12	-0049-20	BLACK PLAIN		
31								1	1	0112-0049-50	KEY TOP RED PLAIN		
32								4	4	0112-0049-40	KEY TOP GREY PLAIN		
33								2	2	0112-0049-30	KEY TOP WHITE PLAIN		

NOTE:

LIST OF MATERIAL
ASSY. KEYBOARD

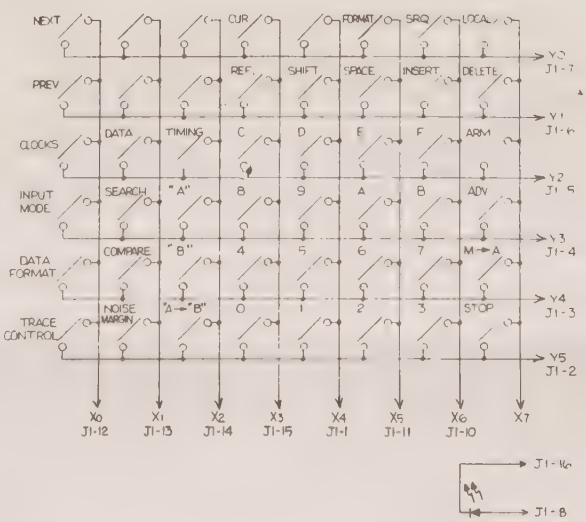
GOULD biomation

B 0117-0040 REV B

MODEL K105 SHEET 2 OF 2

KLINGLER H-VEL H 10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN #316	STM		2-3
	51	—	REV SKIPPED	MW		4-15
	52	3739	REV'D PER ECO	MW	DGW	5/3/83
	A	3957	PROD REL PER ECO No	JWC	DGW	4/6/83
	B	4220	PER ECO	[illegible]	DGW	1/17/84



50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = ± ANGLES; XX = ± .020 ± 1; XXX = ± .010

HOLE SIZE: 0 .599 .003; .600 .999 .004; 1.000 1.499 .005

DASH NO	NUMBER	QTY
10	0117-0040	1

NEXT ASSEMBLY

ENG SERV: R. Gibson — DATE: 2/10/83

DRAWN: [illegible] — DATE: 10/12/80

CHECKED: R. Wood — 2-15-83

PROJ ENG: [illegible] — 2-18-83

MANUFACTURING: [illegible] — 2-18-83

QUALITY ASSUR

GOULD biomation

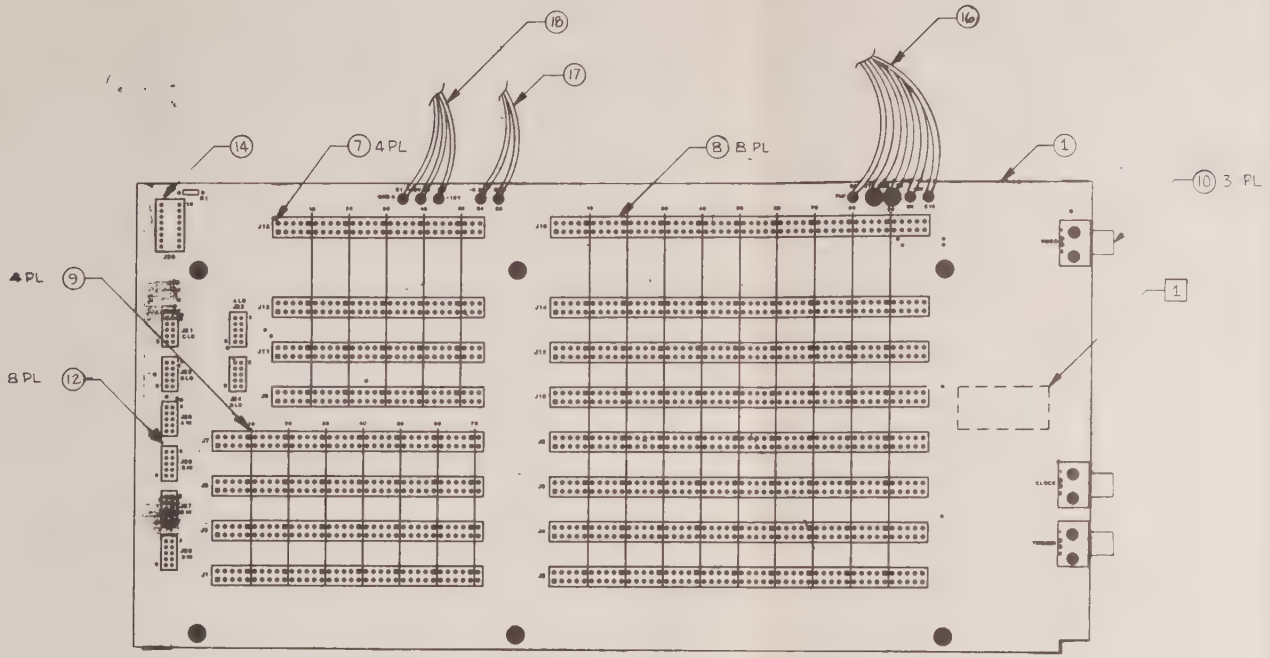
TITLE: SCHEMATIC KEYBOARD, K105

SCALE: — | SIZE: C | PART NUMBER: 0117-0041 | REV: B

CODE: K FRUGAL | SHEET 1 OF 1

0117-0041

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	03		PROTOTYPE	MW		
	50		ENGR RELEASE			
	A	4391	PROD REL PER ECO	D.C		4/16/84



COMPONENT SIDE

NOTES UNLESS OTHERWISE SPECIFIED

1. STAMP ASSEMBLY DASH NO., REVISION LEVEL AND SERIAL NO. APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK.
2. ASSEMBLY REFLECTS SCHEMATIC DRAWING 0117-0046 AND FABRICATION DRAWING 0117-0047.

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL X = 1 ANGLES XX = .020 ± 1° XXX = .010 | HOLE SIZE 0.599 - .003 .000 .999 - .004 1.000 1.499 - .005

ENG SERV | DATE

DASH NO	NUMBER	QTY
10	0117-0010	1
	NEXT ASSEMBLY	

DRAWN H WOLFE DATE 1/13/83

CHECKED R Wood 5/3/83

PROJ ENG [signature] 5/3/83

MANUFACTURING [signature] 5/3/83

QUALITY ASSUR [signature] 5/13/83

GOULD Instruments Division Santa Clara Operations

TITLE ASSEMBLY MOTHER BOARD K105

SCALE 1/1 | SIZE D | PART NUMBER 0117-0045 | REV A

MODEL K105 | SHEET 1 OF 1

ITEM	-90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION
1									1	0117-0047-10	FABRICATION, P.C.B. MOTHERBD	
2									REF	0117-0046-10	SCHEMATIC	
3												
4												
5									1	3000-3300-10	RESISTOR, 330Ω, 5%, CAR	R1
6												
7									4	6000-0198-10	CONN, DUAL 28, PC	J9,11,13,15
8									8	6000-0333-10	CONN, 50 PIN DUAL PC	J2,4,6,8,10,12,14,16
9									4	6000-0333-20	CONN, 36 PIN DUAL PC	J1,3,5,7
10									3	6000-0394-10	CONN, BNC RT. ANGLE	
11												
12									8	6000-0552-20	CONN, 5 PIN DUAL, R. ANGLE	J21,22,23,24,25,26,27,28
13												
14									1	6100-0120-10	SKT 16 PIN DIP LO-PROFILE	J20
15												
16									1	[illegible]-0144-[illegible]	[illegible] MOTHER BD CABLE	
17									1	0117-0221-10	MOTHER BD CABLE 5.2V	
18									1	0117-0222-10	MOTHER BD CABLE 15V	

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL 4391	2-15-84		
[illegible]	[illegible] RELEASE	1-[illegible]-83		
03	PROTOTYPE			

DASH NO.	NEXT ASSEMBLY NUMBER	QTY
10	0117-0010	

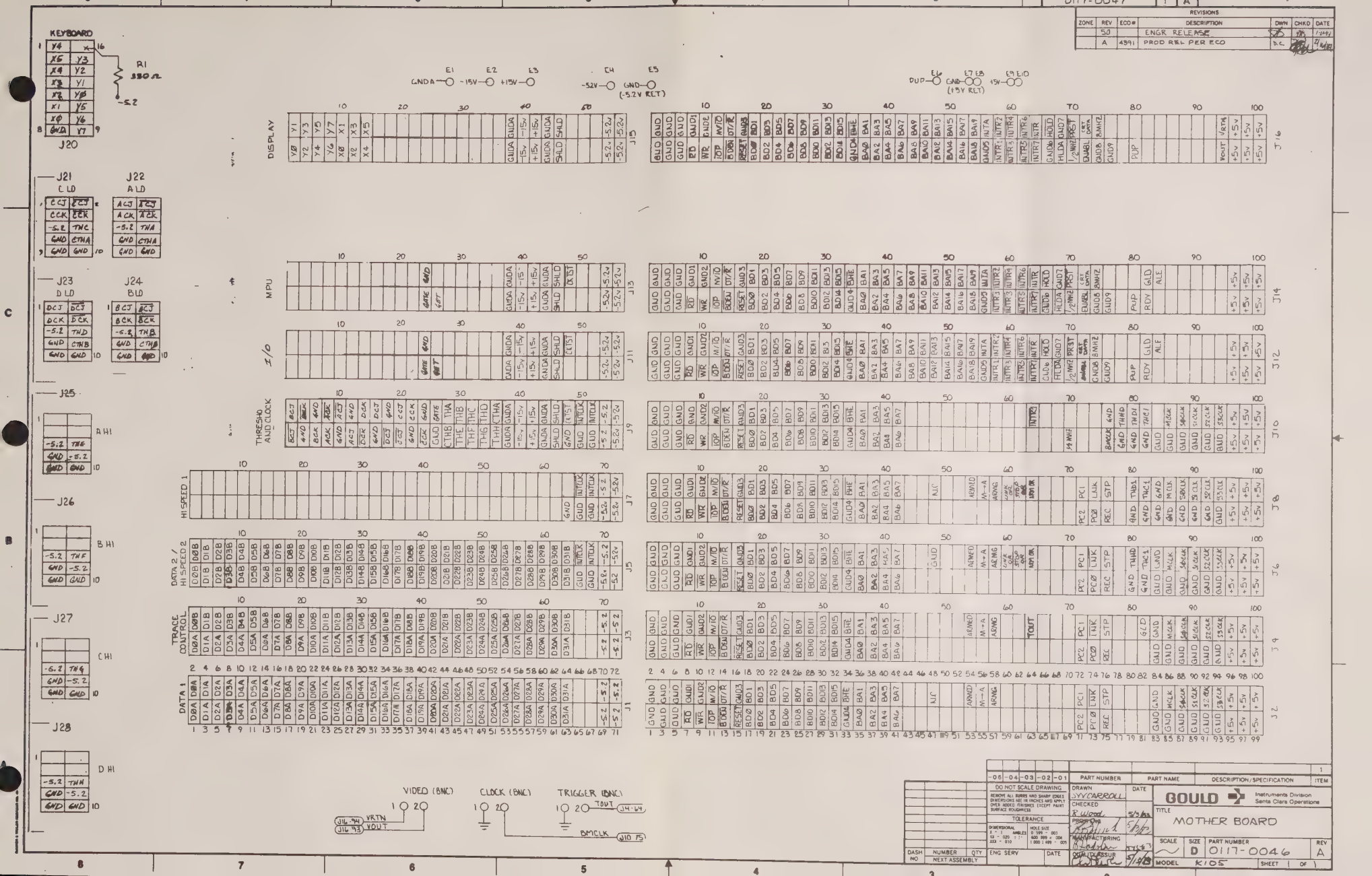
		DATE
DWN	M.WOLFE	1-13-83
CHK	[illegible]	5/3/83
ENGR	[illegible]	[illegible]
MFG.	[illegible]	5/13/83
Q.A.	[illegible]	5/13/[illegible]

LIST OF MATERIAL
ASSEMBLY
MOTHER BOARD

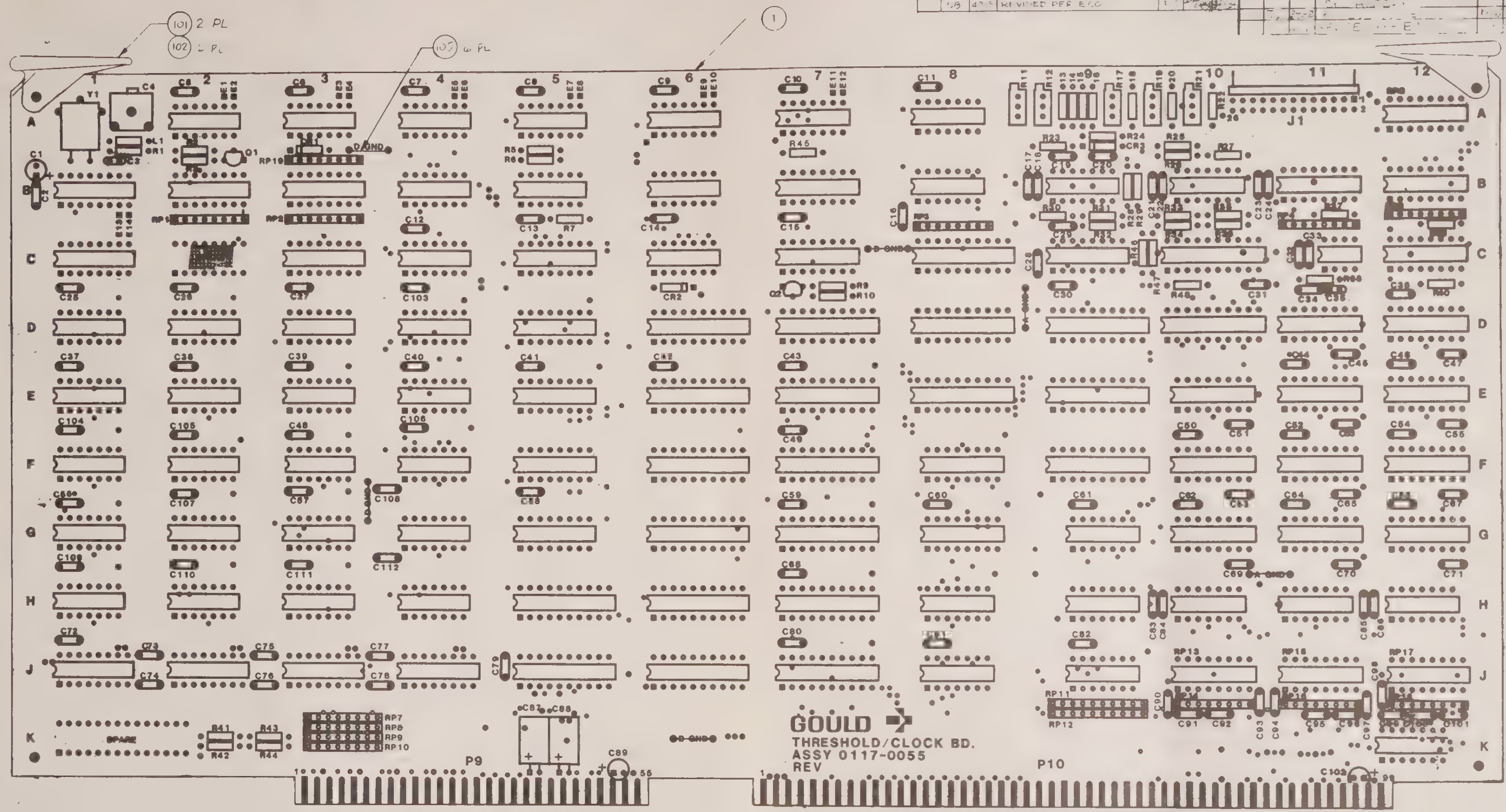
GOULD biomation

B 0117-0045 REV A

MODEL K,05 SHEET 1 OF 1



REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
50 | | ENGR RELEASE
A | 4391 | PROD REL PER ECO
KEYBOARD
J20
R1 330Ω
-5.2
J21 C LD
J22 A LD
J23 D LD
J24 B LD
J25 A HI
J26 B HI
J27 C HI
J28 D HI
DISPLAY
MPU
I/O
THRESHO AND CLOCK
HI SPEED 1
DATA 2 / HI SPEED 2
TRACE CONTROL
DATA 1
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
J16
VIDEO (BNC)
CLOCK (BNC)
TRIGGER (BNC)
VRTN
VOUT
TOUT
BMCLK
J16-94
J16-93
J14-64
J10-75
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
MANUFACTURING
QUALITY ASSUR
GOULD
Instruments Division
Santa Clara Operations
TITLE
MOTHER BOARD
SIZE
D
PART NUMBER
0117-0046
REV
A
MODEL
K105
SHEET 1 OF 1



COMPONENT SIDE

DASH NO	NUMBER	QTY
-10	0117-0003	
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL		HOLE SIZE
X ± .1	ANGLES	0 .599 ± .003
XX ± .020	± 1°	.600 .999 ± .004
XXX ± .010		1.000 1.499 ± .005

ENG SERV | DATE

DRAWN	G. Galindo	7-21-82
CHECKED		
PROD ENG		
MANUFACTURING		
QUALITY ASSUR		

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

GOULD biomation

TITLE ASSEMBLY THRESHOLD/CLOCK PWB

SCALE	SIZE	PART NUMBER	REV
2/1	D	0117-0055	58

CODE K105 | SHEET 1 OF 1

ITEM	-90	-80	-70	-60	-50	-40	-30	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1								—	1	0117-0057-10	PWB, THRESHOLD CLOCK		
2								—	REF	0117-0056	SCHEMATIC, THRESHOLD/CLOCK		
3								1	—	0117-0055-05	THRESHOLD CLOCK		
4								—	1	6100-0121-10	SOCKET, 20 PIN DIP	X 10C	
5								—	1	6100-0120-10	SOCKET, 16 PIN DIP, LP	X 9C	
6													
7													
8								—	2	1800-0409-10	I.C 74F00	3D, 4D	
9								—	2	-0107-10	74LS04	8A 2A	
10								—	3	-0538-10	74F08	2D, 1D, 12K	
11								—	1	-0110-10	74LS10	9G	
12								—	3	-0123-10	74LS14	8H, 9H, 9J	
13								—	2	-0215-10	74LS27	8J 5B	
14								—	3	-0365-10	74LS28	4C, 4B 8B	
15								—	16	-0537-10	74F64	1F, 2F, 1H, 2H, 3H, 4H, 1G, 2G, 3G, 4G, 3F, 4F, 1E, [illegible]E, 3E, 4E	
16								—	7	-0118-10	74LS90N	3A, 4A, 5A, 6A, 7A, 6B, 6C	
17								—	2	-0193-10	74LS38N	8G 8F	
18								—	1	-0525	74F244	5H	
19								—	4	-0240-10	74LS244N	6E 9E, 5J [illegible]	
20								—	6	-0360-10	74F251	5D 5E 5F, 5G, 7B, 7C	
21								—	1	-0554-10	74F251	5C	
22								—	[illegible]	[illegible]-0231-10	74LS[illegible]3	[illegible] 9F 4D, 6J [illegible] 6E, 6H 6F 6D J [illegible] [illegible] 7F, 7E	
23													
24													
25								—	1	1850-[illegible]-10	MC10[illegible]	1B	
26								—	1	[illegible]-10	MC [illegible]05	3C	
27								—	1	[illegible]-10	I.C MC10121	[illegible]B	

REV	DESCRIPTION	DATE	DWN	CKD
—	SEE HISTORY	[illegible]	[illegible]	[illegible]
55	REL ECO #3-42[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	REL ECO #3-4[illegible]	[illegible]	[illegible]	[illegible]
57	REL ECO #4050	[illegible]	[illegible]	[illegible]
57K	REL ECO 4264	1-23-84	[illegible]	[illegible]
58	PER ECO 4315	2-21-84	D.C	[illegible]

DASH NO.	NEXT ASSEMBLY NUMBER	QTY
10	0117-0003-10	1

		DATE
DWN	[illegible]	[illegible]
CHK	[illegible]	[illegible]
ENGR	[illegible]	[illegible]
MFG.	[illegible]	[illegible]
Q.A.	[illegible]	[illegible]

LIST OF MATERIAL
ASSEMBLY
THRESHOLD/ CLOCK
PWB

GOULD biomation

B | 0117-0055 | REV 58
MODEL K105 | SHEET 1 OF 4

KLINGLER K-VEL H10

ITEM	-90	-80	-70	-60	-50	-40	-30	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
								—	4	1850-0014-10	I.C. MC 10125	1J 2J, 3J, 4J	
								—	1	1850-[illegible] 10	MC [illegible]131	1C	
								—	1	1850-[illegible]041-10	MC 10138	2B	
								—	5	1700-0086-10	324A	9B, 10H 11H 12H [illegible]B	
								—	1	1700-0071-10	LF356N	11C	
								—	3	1820-[illegible]-10	MP 7528 DIJN	11B, 12B 12C	
								1	—	1900-[illegible]014-10	ADC1001	10C	
								1	—	1900-0012-10	DAC 8	9C	
								—	11	1820-[illegible]052-10	I.C 4051B	10E, 10F, 10G, 11D, 11E, 11F, 11G, 12D, 12E, 12F, 12G	
								—	2	1400-[illegible] 10	TRANSISTOR, 2N3906	Q1, 2	
								—	1	1100-0015-10	DIODE, 6.2V, IN825A	CR3	
								—	2	1000-0002-10	DIODE, IN4152	CR1, 2	
								—	1	2100-0040-10	INDUCTOR, FERRITE CORE, 0.15	L1	
								—		5100-0024-10	CRYSTAL, .39uh, [illegible] MHz	Y1	
								—	3	3100-[illegible]001-10	RESISTOR 1K 1/8W, 1%, MF	R3[illegible] 39 40	
								—	2	-3321 10	3.32K	R13, 30	
								—		-3531 10	5.53K	R[illegible]1	
								—	[illegible]	3100-3741-10	RESISTOR 3.74K, 1/8W, 1%, MF	R 32	

LIST OF MATERIAL
ASSEMBLY
THRESHOLD/CLOCK PWB

GOULD biomation

B | 0117-0055 | REV 58
MODEL K105 | SHEET 2 OF 4

KLINGLER K-VEL H10

ITEM	QUANTITY PER ASSEMBLY -60	-80	-70	-60	-50	-40	-30	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
58													
59								—	4	3100-1002-10	RESISTOR, 10K, 1/8W, 1%, MF	R16, 18, 23, 24	
60								—	1	3100-2002-10	20K,	R20	
61								—	1	3100-1212-10	12.1K,	R34	
62								—	1	3100-1242-10	12.4K, 1/8W 1% MF	R33	
63								—	8	3000-5106-10	51, 1/4W, 5% CAR	C14 5 2 .0 36 25 27	
64								—	2	-1000-10	100.	C42 44	
65								—	1	-1500-10	150,	R43	
66								—	1	-1800-10	180,	R5	
67								—	2	-2000-10	200,	R3 9	
68								—	3	-4701-10	4.7K	R46 47 48	
69								—	1	-2700-10	270.	R6	
70								—	1	-3300-10	330.	R29	
71								—	1	-5100-10	510.	R1	
72								—	2	-8200-10	820	R7, 28	
73								—	2	3000-6201-10	6.2K 1/4W .5% CAR	R35 45	
74								—	1	3000-2401-10	2.4K, 1/4W, 5%	R38	
75								—	1	3100-7501-10	RESISTOR, 7.5K, 1/8W, 1%	R22	
76								—	1	3000-1201-10	RESISTOR 120 1/4W, 5% C	R49	
77								—	1	3300-0115-10	POT 2K .25W 10% 12T	RC1	
78								—	2	3300-0012-10	POT, 1K, .5W, 1[illegible] 20T	R11 2	
79								—	2	3300-0011-10	POT, 10K, .5W, 10% 25T	R17, 19	
81								—	1	3700-0026-10	RES PAK 120, .3W 2%, 8 PIN	RP9	
82								—	2	3700-0096-10	RES PACK 100 .2W .1% 8 PIN	RP10	
83								—	1	3700-0102-10	RESISTOR, 150 .2W 2% 8/78	RP[illegible]	
84								—	3	3700-0136-10	RESISTOR, 56 2% 8/78	R[illegible] 18	
85								—	2	3700-0021-10	R. PAK, 470 .3W 2% 8 PIN	RP12	
86								—	1	3700-0124-10	R. PAK, 1K .2W 1% 8 PIN	RP6	
87								—	1	3700-0057-10	[illegible] .18W .1% 8 PIN	RP5	
88								—	2	3700-0051-10	RES PACK 0K, 2W, 2% 8 PIN	RP4 6	

NOTES

LIST OF MATERIAL
ASSEMBLY
THRESHOLD / CLOCK PWB

GOULD ⇒ biomation
B | 017-0055 | REV 58
MODEL K105 | SHEET 3 OF 4

KLINGLER K-VEL H 10

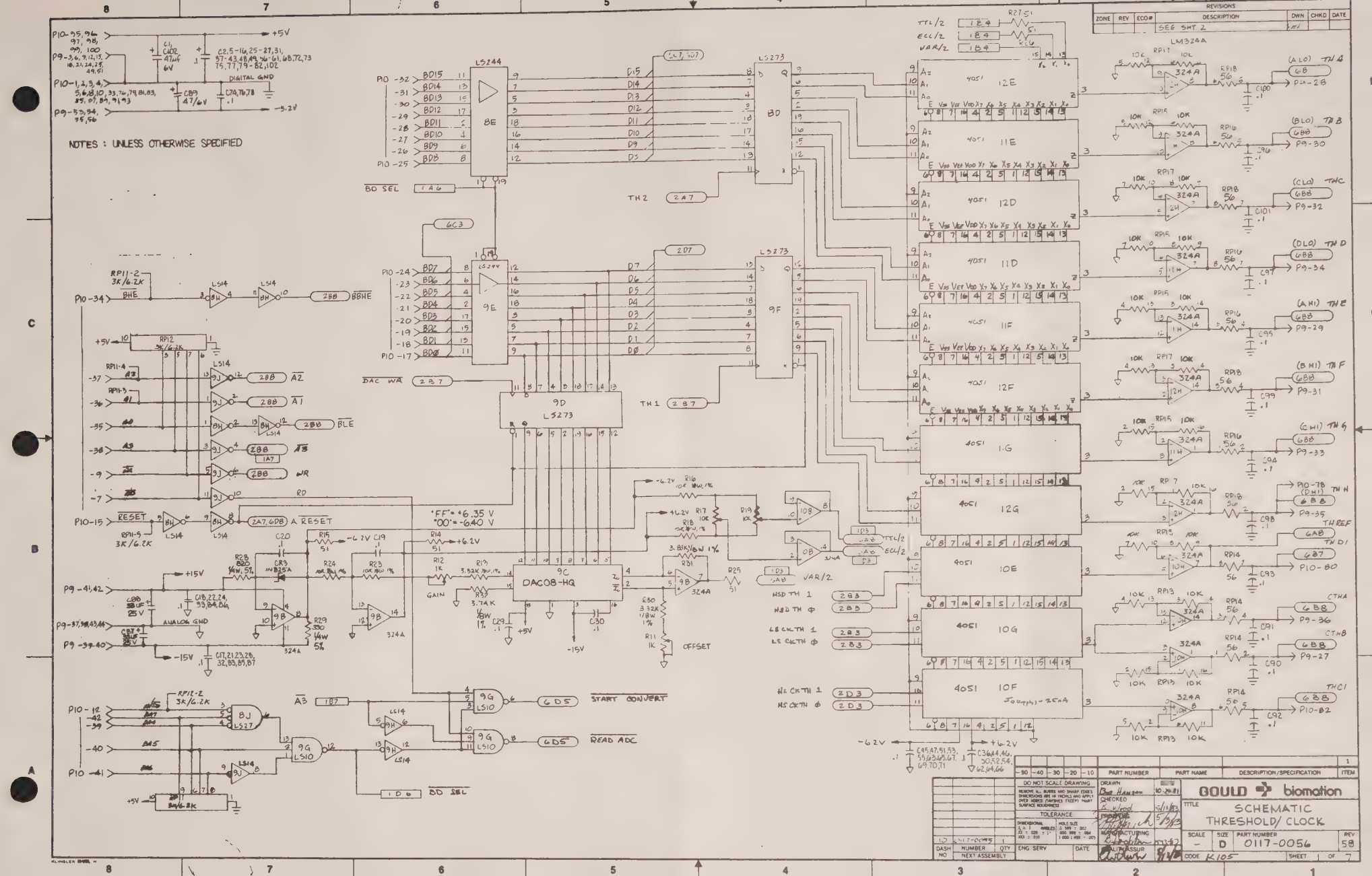
ITEM	QUANTITY PER ASSEMBLY -60	-80	-70	-60	-50	-40	-30	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
89								—	3	3700-0048-10	RES PACK 1K .2W 16 PIN	RP13 15 17	
90								—	2	3700-0049-10	RES PACK 4K .2W 16 PIN SIP	RP 11 12	
91								—	1	3700-0041-10	RES PACK 4.7K 2W, 2%, 8 PIN	RP19	
92													
93								—	1	4010-0102-20	CAPACITOR .02 1[illegible] 1000V 5%	C3	
94								—	104	4[illegible]-0025-10	.1 [illegible] 100%	C 5-34 36 [illegible] 103-112	
95								—	3	4[illegible]-0042-10	47 [illegible]	C[illegible]	
96								—	2	4400-0045-10	33 [illegible] 25V	C8 [illegible]	
97								—	1	4000-0040-10	CAPACITOR 470 µf, 50V, 10%	C35	
98													
99								—	1	4[illegible]-0025-10	CAP .1 µf, 100V	C4	
100													
101								—	2	7[illegible]-0120-10	CARD EJECTOR, NYLON white		
102								—	4	7000-0412-10	CARD EJECTOR, PIN 3/32 x 1/4		
103								—	1	[illegible]-0[illegible]-10	CONN. HDR, RT ANGLE, 76 PIN	J1	
104													
105								—	6	9000-0054-10	BUSS WIRE, INSULATED	[illegible] GND	
106													
107													
108													
109													
110													
111													
112													
113													
114													
115													
116													
117													
118													

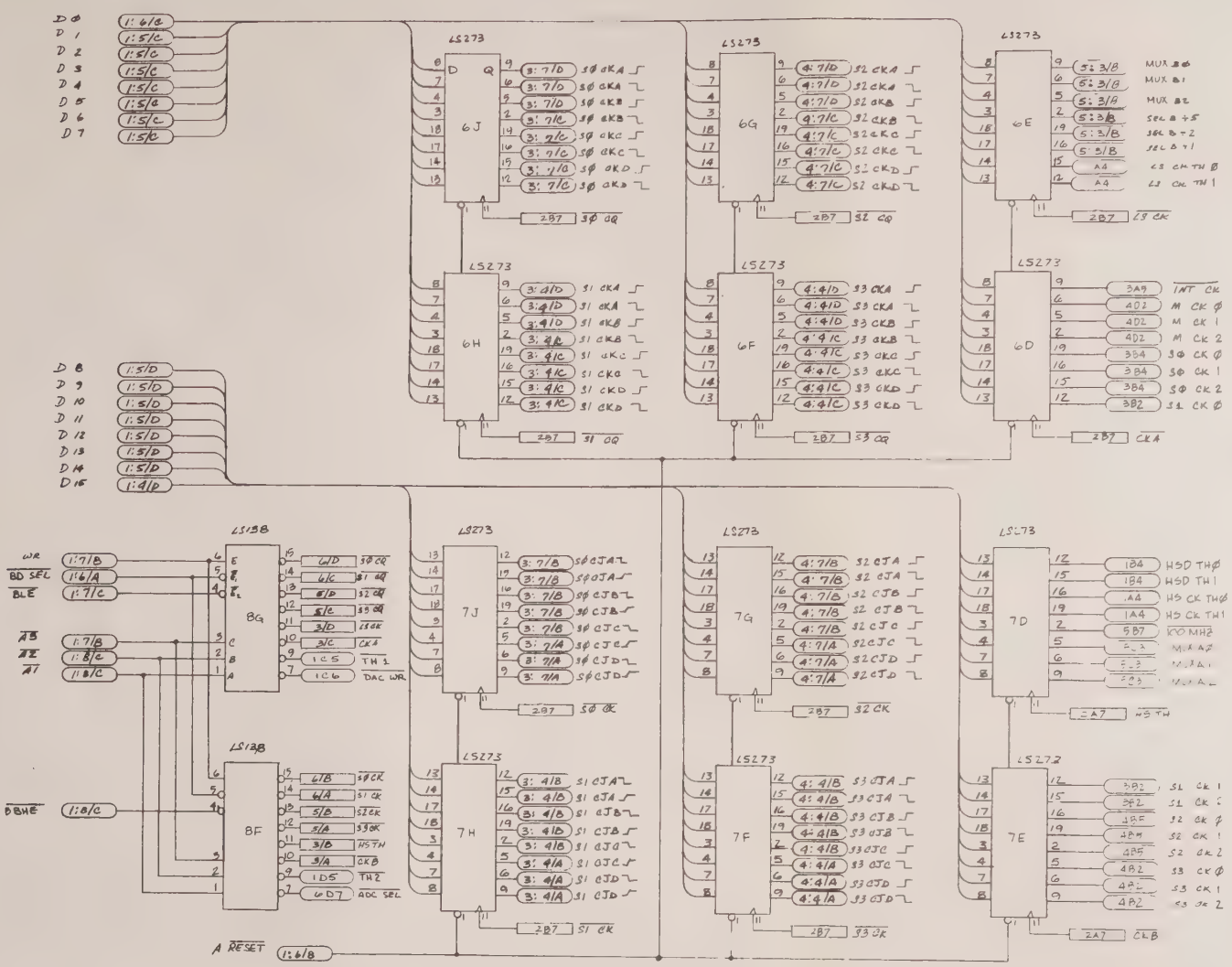
NOTES

LIST OF MATERIAL
ASSEMBLY
THRESHOLD / CLOCK PWB

GOULD ⇒ biomation
B | 017-0055 | REV 58
MODEL K105 | SHEET 4 OF 4

KLINGLER K-VEL H 10


NOTES : UNLESS OTHERWISE SPECIFIED
DIGITAL GND
ANALOG GND
LS244
8E
9E
LS273
8D
9F
9D
LS273
9C
DAC08-HQ
4051
12E
11E
12D
11D
11F
12F
1G
12G
10E
10G
10F
LM324A
BD SEL
DAC WR
TH 2
TH 1
"FF" = +6.35 V
"00" = -6.40 V
GAIN
OFFSET
START CONVERT
READ ADC
BD SEL
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
SEE SHT 2
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJECT
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCHEMATIC
THRESHOLD/ CLOCK
SCALE
SIZE
D
PART NUMBER
0117-0056
REV
58
CODE K105
SHEET 1 OF 7



ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	01		RELTO			
	02		REVISED 11-8-82			
	03		REVISED 1-11-83			
	04		REVISED PER ECN 1230, 1241			
	50		RELTO REL PER ECN 349			
	51		CCB ERROR	—	—	—
	52	3890	REVISED PER ECO	MW		
	53	3908	REVISED PER ECO	MW		
	54	3924	REVISED PER ECO	MW		
	55	3943	REVISED PER ECO	MW		
	56	3962	REVISED PER ECO	MW		
	57	4050	REVISE PER ECO	SAR		
	58	4315	REVISE PER ECO	DC		

DWG. NO. 0117-0056 SH. 2 REV 58

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DO NOT SCALE DRAWING

TOLERANCE

ENG SERV DATE

DRAWN DATE

CHECKED

PROJ ENG

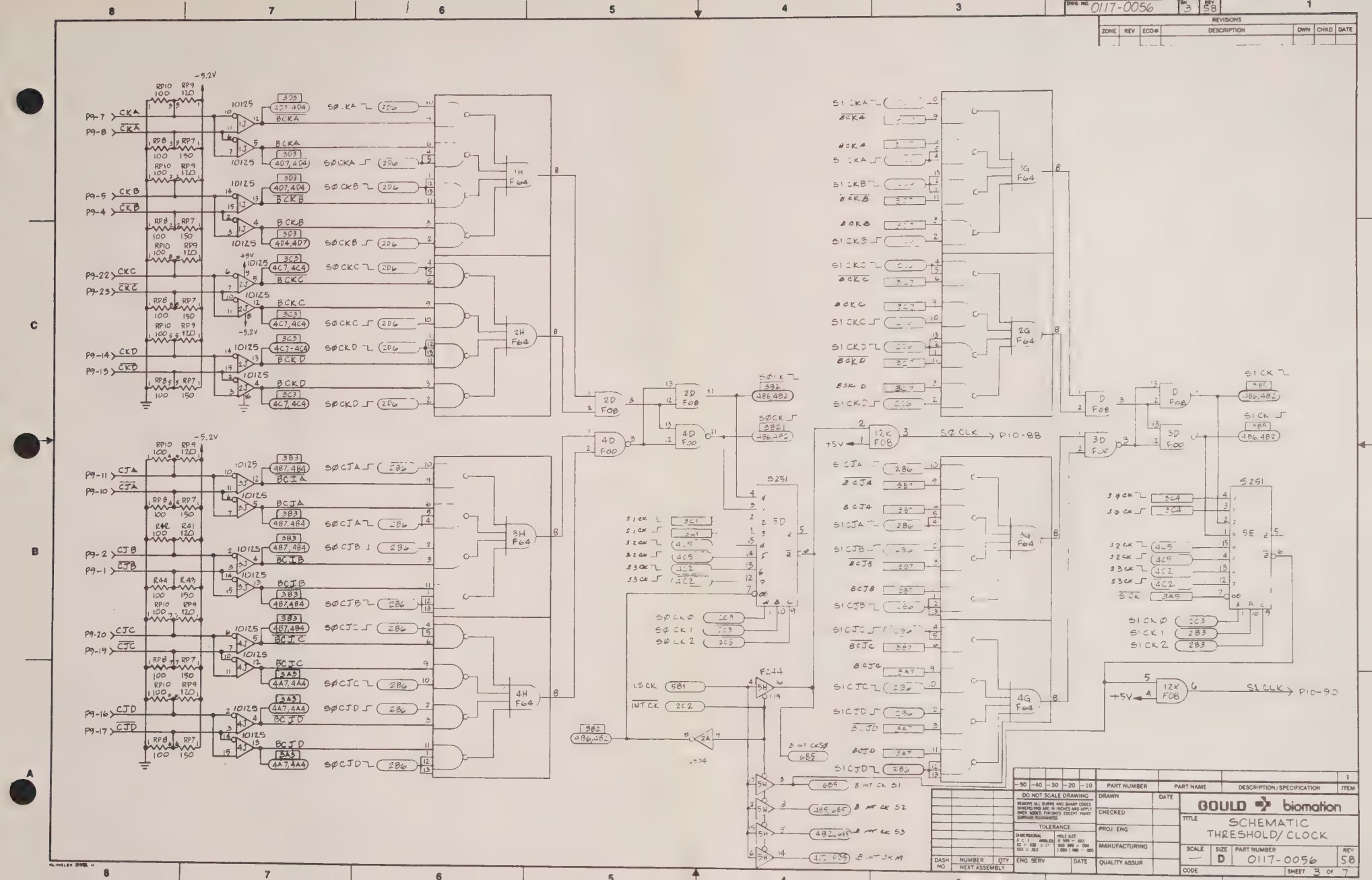
MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE SCHEMATIC THRESHOLD/CLOCK

SCALE — SIZE D PART NUMBER 0117-0056 REV 58



DWG. NO. 0117-0056
SH. 3
REV. 58
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
P9-7 CKA
P9-8 CKA
P9-5 CKB
P9-4 CKB
P9-22 CKC
P9-23 CKC
P9-14 CKD
P9-13 CKD
P9-11 CJA
P9-10 CJA
P9-2 CJB
P9-1 CJB
P9-20 CJC
P9-19 CJC
P9-16 CJD
P9-17 CJD
-5.2V
+5V
10125
1H F64
2H F64
3H F64
4H F64
1G F64
2G F64
3G F64
4G F64
2D F08
4D F00
12K F08
D F08
3D F00
S251
5D
5E
F244
S1 CLK
P10-88
P10-90
S1 CK
S2 CK
S3 CK
S1 CK0
S1 CK1
S1 CK2
LS CK
INT CK
B INT CK S1
B INT CK S2
B INT CK S3
B INT CKM
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
TOLERANCE
DIMENSIONAL
ANGLES
HOLE SIZE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
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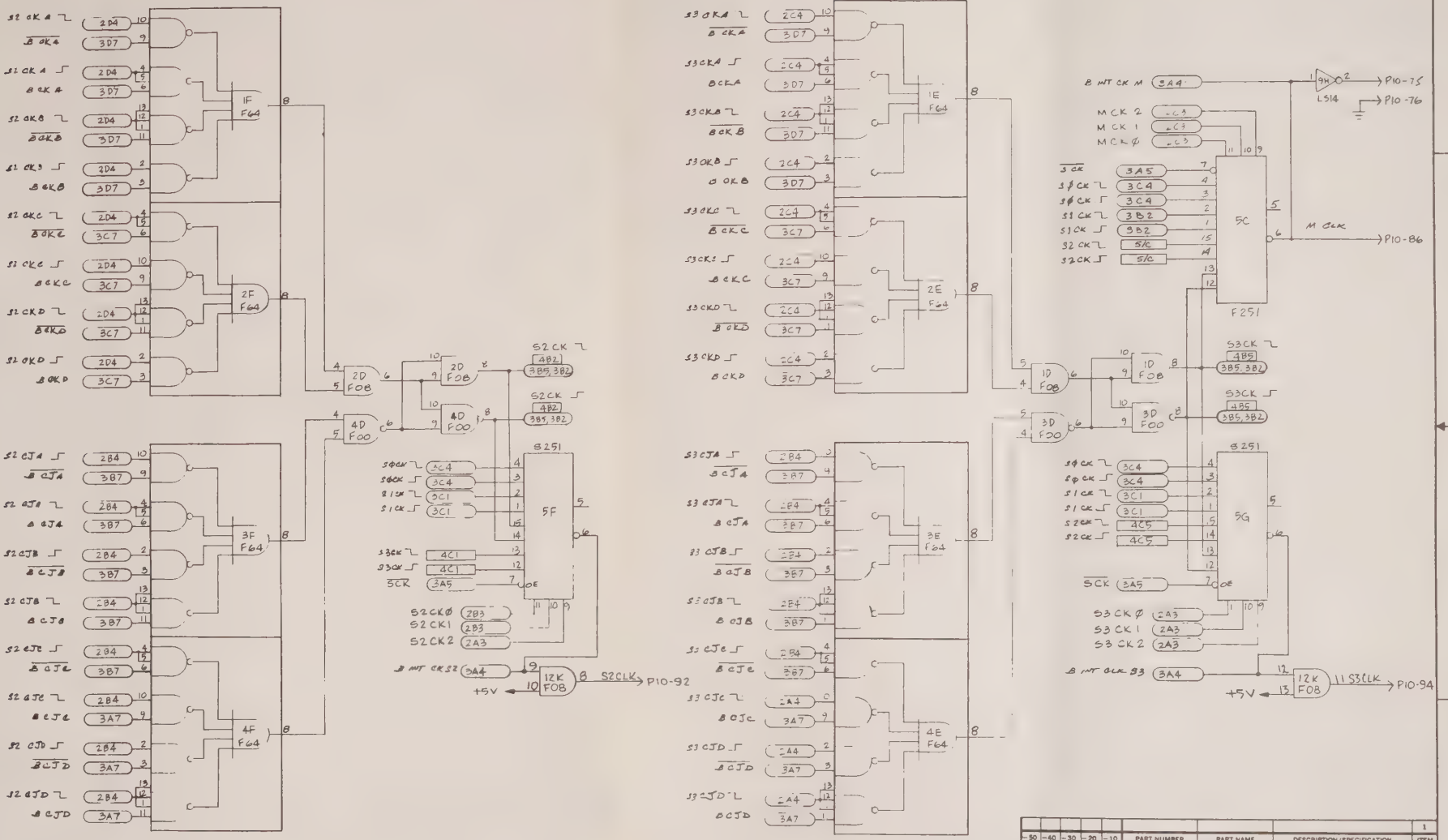
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE
SCHEMATIC
THRESHOLD/CLOCK
SCALE
SIZE
D
PART NUMBER
0117-0056
REV
58
CODE
SHEET 3 OF 7



ZONE	REV	ECO #	REVISIONS DESCRIPTION	DWN	CHKD	DATE

DASH NO	NUMBER	QTY	NEXT ASSEMBLY
			ENG SERV DATE

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

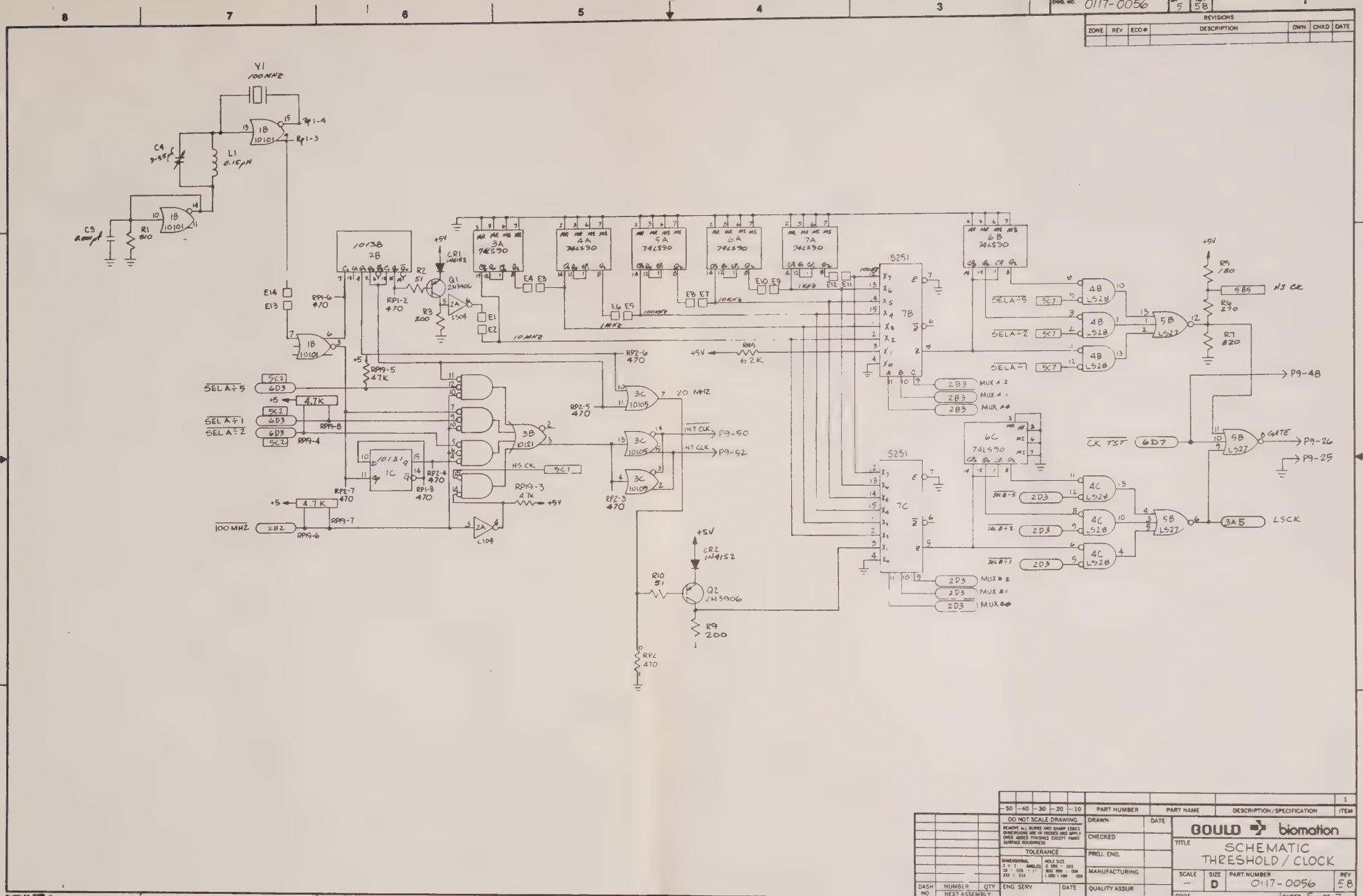
DRAWN DATE
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR

GOULD biomation

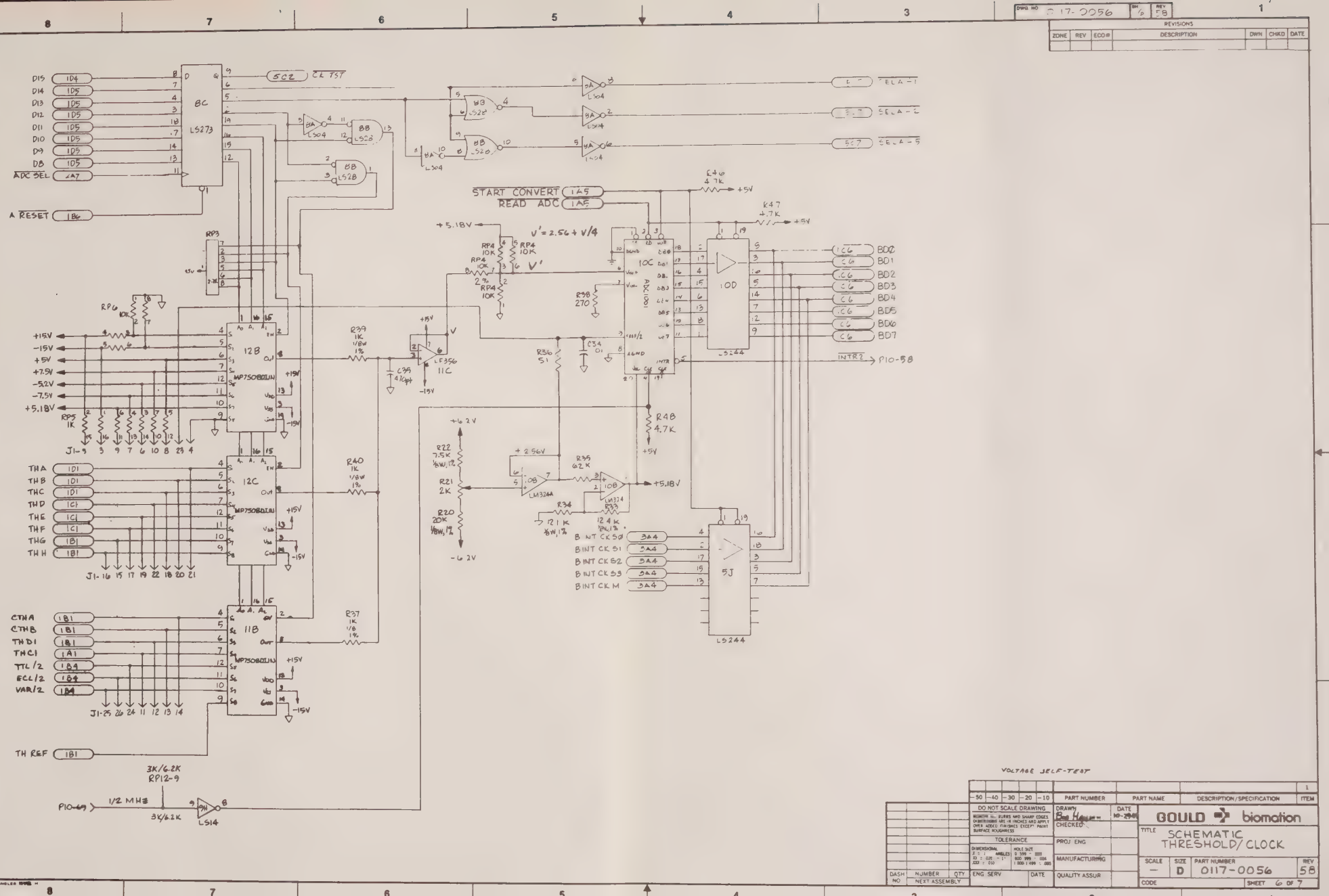
TITLE SCHEMATIC THRESHOLD/CLOCK

SCALE	SIZE	PART NUMBER	REV
—	D	0117-0056	5B

CODE SHEET 4 OF 7



DWG. NO. 0117-0056 5 58
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
Y1 100MHZ
C4 9-35pf
L1 0.15μH
C3 0.001μf
R1 510
1B 10101
Rp1-4
Rp1-3
10138 2B
CR1 1N4152
Q1 2N3906
R2 51
R3 200
LS04
E14
E13
RP1-6 470
RP1-2 470
E1
E2
10MHZ
3A 74LS90
4A 74LS90
5A 74LS90
6A 74LS90
7A 74LS90
6B 74LS90
E4 E3
E6 E5
E8 E7
E10 E9
E12 E11
1MHZ
100KHZ
10KHZ
1KHZ
S251 7B
S251 7C
6C 74LS90
RP2-6 470
R45 62K
+5V
RP19-5 47K
SEL A÷5
SEL A÷1
SEL A÷2
5C2
6D3
4.7K
RP19-8
RP19-4
3B 10121
3C 10105
20 MHZ
RP2-5 470
INT CLK
P9-50
P9-52
HS CK
5C1
10131 1C
RP2-4 470
RP1-8 470
RP2-7 470
RP19-3 4.7K
RP2-3 470
100MHZ
2B2
RP19-7
RP19-6
CR2 1N4152
R10 51
Q2 2N3906
R9 200
RV2 470
2B3 MUX A 2
2B3 MUX A 1
2B3 MUX A0
2D3 MUX B 2
2D3 MUX B1
2D3 MUX B0
SEL A-5
SEL A-2
SEL A-1
5C7
4B LS28
5B LS27
R5 180
5B5 HS CK
R6 270
R7 820
P9-48
CK TST
6D7
GATE
P9-26
P9-25
4C LS28
3A5 LSCK
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL
HOLE SIZE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE
SCHEMATIC THRESHOLD / CLOCK
SCALE
SIZE D
PART NUMBER 0117-0056
REV 5B
CODE
SHEET 5 OF 7



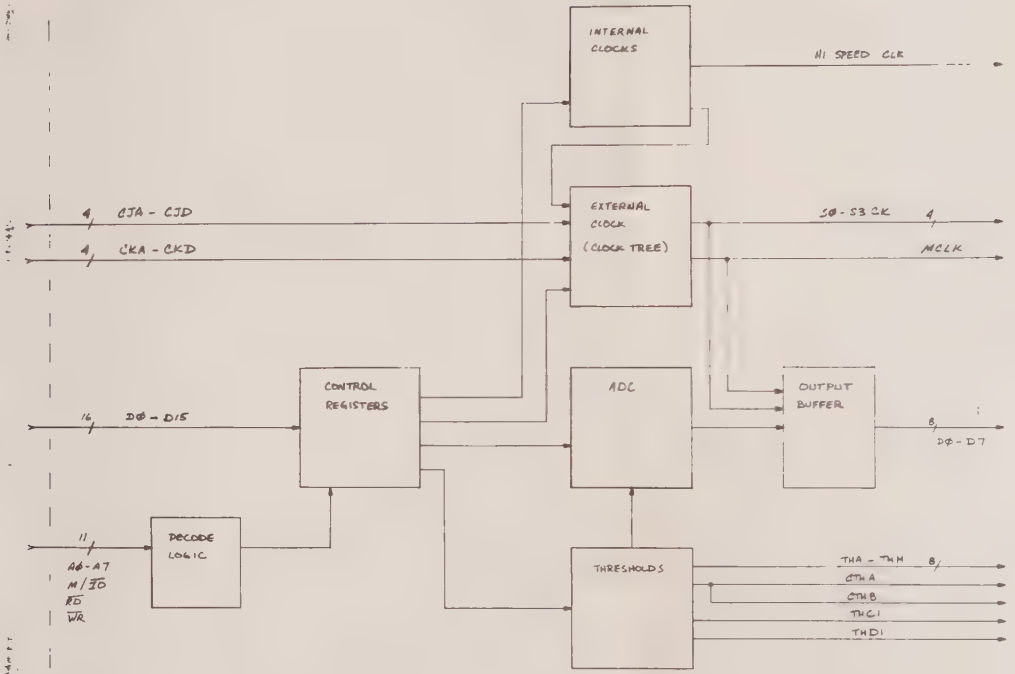
DWG NO 0117-0056
SH 6
REV 58
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
D15 1D4
D14 1D5
D13 1D5
D12 1D5
D11 1D5
D10 1D5
D9 1D5
D8 1D5
ADC SEL 2A7
A RESET 1B6
8C LS273
5C2 CK TST
8A LS04
8B LS28
SELA-1
SELA-2
SELA-5
START CONVERT 1A5
READ ADC 1A5
R46 4.7K
R47 4.7K
+5V
+5.18V
V' = 2.56 + V/4
RP4 10K
RP4 10K
RP4 10K
RP4 10K
2%
V'
10C ADC1001
10D LS244
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
INTR2 P10-58
R38 270
R36 51
C34 .01
R48 4.7K
RP3
RP6 10K
+15V
-15V
+5V
+7.5V
-5.2V
-7.5V
+5.18V
RP5 1K
J1-9 3 9 7 6 10 8 23 4
12B MP7508DIJN
12C MP7508DIJN
11B MP7508DIJN
R39 1K 1/8W 1%
R40 1K 1/8W 1%
R37 1K 1/8 1%
C35 470pf
LF356 11C
THA 1D1
THB 1D1
THC 1D1
THD 1C1
THE 1C1
THF 1C1
THG 1B1
THH 1B1
J1-16 15 17 19 22 18 20 21
CTHA 1B1
CTHB 1B1
THD1 1B1
THC1 1A1
TTL/2 1B4
ECL/2 1B4
VAR/2 1B4
J1-25 26 24 11 12 13 14
TH REF 1B1
+6.2V
-6.2V
R22 7.5K 1/8W,1%
R21 2K
R20 20K 1/8W,1%
+2.56V
R35 62K
10B LM324A
10B LM324
R34 121K 1/8W,1%
R33 124K 1/8W,1%
+5.18V
BINT CK S0 3A4
BINT CK S1 3A4
BINT CK S2 3A4
BINT CK S3 3A4
BINT CK M 3A4
5J LS244
3K/6.2K RP12-9
P10-69
1/2 MHz
3K/6.2K
9H LS14
VOLTAGE SELF-TEST
-50 -40 -30 -20 -10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
DATE
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC THRESHOLD/CLOCK
SCALE —
SIZE D
PART NUMBER 0117-0056
REV 58
CODE
SHEET 6 OF 7

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

K105 MOTHER BD

K105 THRESHOLD / CLOCK BD.

K10E MOTHER BD.



NOTE:
SQUARE PADS —□ □—
DENOTE GEN RAD BREAKPOINTS

-06	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES UNDIMENSIONS ARE IN INCHES AND APPLY OVER ABOVE FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DRAWN DATE
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR

GOULD Instruments Division Santa Clara Operations

TITLE SCHEMATIC
THRESHOLD / CLOCK

SCALE | SIZE D | PART NUMBER 0117-0056 | REV 58

MODEL K105 | SHEET 7 OF 7

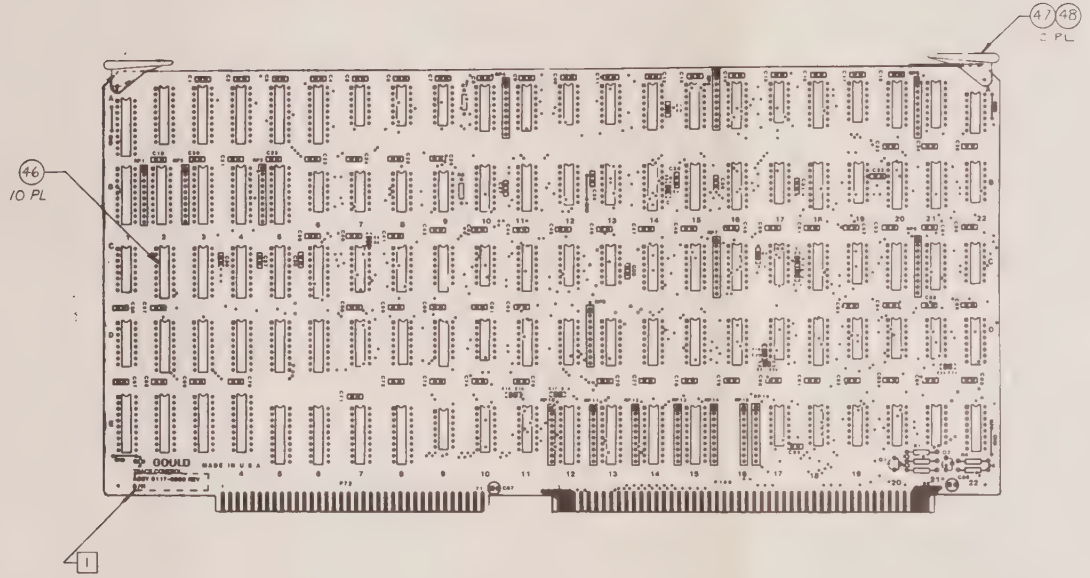
DASH NO	NUMBER NEXT ASSEMBLY	QTY
10	0 7-0055	1

ENG. SERV DATE

DWG NO	SH	REV
0117-0060	1	62

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	02		PROTOTYPE			
	03		PROTOTYPE			
	50	349	PILOT RELEASE			
	56	429	[illegible]	[illegible]	[illegible]	[illegible]
	57	4420	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	58	[illegible]	[illegible]	[illegible]		
	59	[illegible]	[illegible]	[illegible]		
	60	4497	REVISED PER ECO	MW	[illegible]	4-7-84
	61	4543	PER ECO	[illegible]	[illegible]	[illegible]
	62	4563A	REV'D PER ECO 4563A	[illegible]	[illegible]	[illegible]



COMPONENT SIDE

NOTES: UNLESS OTHERWISE SPECIFIED

1 MARK ASSEMBLY DASH NO., REVISION LEVEL AND SERIAL NO. APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK.

-06	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X - 1 ANGLES; XX - .020 ± 1°; XXX - .010

HOLE SIZE: 0.599 - .003; .000 .999 - .004; 1.000 1.999 - .005

DASH NO	NUMBER	QTY
0	0117 0003	1

NEXT ASSEMBLY

ENG SERV | DATE

DRAWN	[illegible]	DATE 2-21-83
CHECKED	R. Wood	5/13/83
ENGINEERING	[illegible]	[illegible]
MANUFACTURING	[illegible]	[illegible]
QUALITY ASSUR	[illegible]	5/13/83

GOULD Instruments Division Santa Clara Operations

TITLE ASSEMBLY TRACE CONTROL

SCALE	SIZE	PART NUMBER	REV
1/1	D	0117-0060	62

MODEL K105 SHEET 1 OF 1

ITEM	QUANTITY PER ASSEMBLY -80	-70	-60	-50	-40	-30	-20	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1								—	1	0117-0062	P.C. BD. TRACE CTL.		
2								—	1	0117-0061	SCHEMATIC TRACE CTL		
								1	—	0117-0060-05	P.W.A. TRACE CTL		
3								—	1	1300-0028-10	TRAN 2N3904	Q2	
4								—	1	1400-0019-10	TRAN 2N3906	Q1	
5								—	1	1800-0031-10	I.C. 74S00	13C	
6													
7								—	5	1800-0038-10	I.C. 74S20	7A,7B,8A,8B,12B	
8								—	3	1800-0039-10	I.C. 74S112	8C,8D,22D	
9								—	3	1800-0059-10	I.C. 74S74N	20D,20E,17B	
10								—	3	1800-0060-10	I.C. 74S10N	10C,19D,17C	
11								—	1	1800-0090-10	I.C. 74B5N	10E	
12								—	4	1800-0092-10	I.C. 74S04N	6B,9C,9D,19E	
13								—	1	1800-0098-10	I.C. 74S134	7D	
14								—	2	1800-0107-10	I.C. 74LS04	9E,12C	
15								—	1	1800-0109-10	I.C. 74LS08	19A	
16								—	1	1800-0121-10	I.C. 74LS175	14D	
17								—	1	1800-0094-10	I.C. 74S175	22E	
18								—	4	1800-0193-10	I.C. 74LS13B	18A,18B,18C,18D	
19								—	3	1800-0204-10	I.C. 74S133	1C,1D,7C	
20								—	3	1800-0226-10	I.C. 74S02	9A,9B,22A	
21								—	4	1800-0243-10	I.C. 74S08	19B,22B,21E,17A	
22								—	4	1800-0244-10	I.C. 74S32	10D,13B,19C,21D	
23								—	1	1800-0253-10	I.C. 74S260	22C	
24								—	5	1800-0268-10	I.C. 74LS245N	1B,2B,3B,4B,5B	
25								—	1	1800-0275-10	I.C. 74LS21	18E	

REV	DESCRIPTION	DATE	DWN	CKD
62	PER ECO 4563A	6/25/82	RTM	
	SEE HISTORY			

DASH NO.	NUMBER	NEXT ASSEMBLY	QTY
10	0117-0003-10		1

		DATE
DWN		11/29/82
CHK	R. Wood	5/13/83
ENGR		5/13/83
MFG.		5/18/83
Q.A.		6/14/83

LIST OF MATERIAL

TRACE CONTROL

GOULD biomation

B 0117-0060 REV 62

MODEL K105 SHEET 1 OF 2

KLINGLER K-VEL M10

ITEM	QUANTITY PER ASSEMBLY -80	-70	-60	-50	-40	-30	-20	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
26								—	1	1800-0106-10	I.C. 74LS02	17E	
27								—	8	1800-0297-10	I.C. 74S374J	1E,2E,3E,4E,5E,6E,7E,8E	
28								—	1	1800-0298-10	I.C 74LS373N	12E	
29								—	5	1800-0554-10	I.C. 74F251	10A,10B,21A,21B,21C	
30													
31								—	1	1800-0362-10	I.C. 74LS366A	11E	
32								10	—	1800-0521-10	I.C. 2149-35	2C,2D,3C,3D,4C,4D,5C,5D,6C,6D	
33								—	7	1800-0572-10	I.C. 74F191	14A,14B,14C,16A,16B,16C,16D	
34								—	1	1800-0523-10	I.C. 74S85	13D	
35								—	12	1800-0524-10	I.C. 74F189	11A,11B,11C,11D,12D,15A,15B,15C,15D,20A,20B,20C	
36								—	3	1800-0525-10	I.C. 74F244	13E,14E,15E	
37													
38								—	1	3000-1001-10	RES 1K, 1/4W, 5%, CAR	R5	
39								—	1	3000-2000-10	RES 20	R3	
40								—	4	3000-4700-10	RES 470	R1,R4,R7,R8	
41								—	1	3000-5106-10	RES 51, 1/4W, 5%, CAR.	R2	
42								—	4	3700-0049-10	RPAK 3K/6.2K 10 PIN	RP12,RP13,RP15,RP16	
43								—	12	3700-0075-10	RPAK 4.7K 10 PIN	RP1,RP2,RP3,RP4,RP5,RP6,RP7,RP8,RP9,RP10,RP11,RP14	
44								—	85	4010-0103-10	CAP .01UF 100V, 10%	C1 - C85	
45								—	2	4400-0043-10	CAP 47 UF 6V	C86,C87	
46								—	10	6100-0146-10	SKT 18 PIN	2C,2D,3C,3D,4C,4D,5C,5D,6C,6D	
47								—	2	7000-0912-10	CARD EJCT. PIN	—	
48								—	2	7000-0120-10	CARD EJCT.	—	
49								—	5	9000-0059-10	BUSS WIRE FORMED		
50													
51								—	1	1800-0535-10	I.C. 74F11	12A	
52								—	1	1800 0534 10	I.C. 74F10	17D	
53													
54								—	1	4010-0101-10	CAP 100PF	C88	
55								12	12		BUSS WIRE, 22 AWG, 1/2" LONG	E POINTS	

NOTES

LIST OF MATERIAL

TRACE CONTROL

GOULD biomation

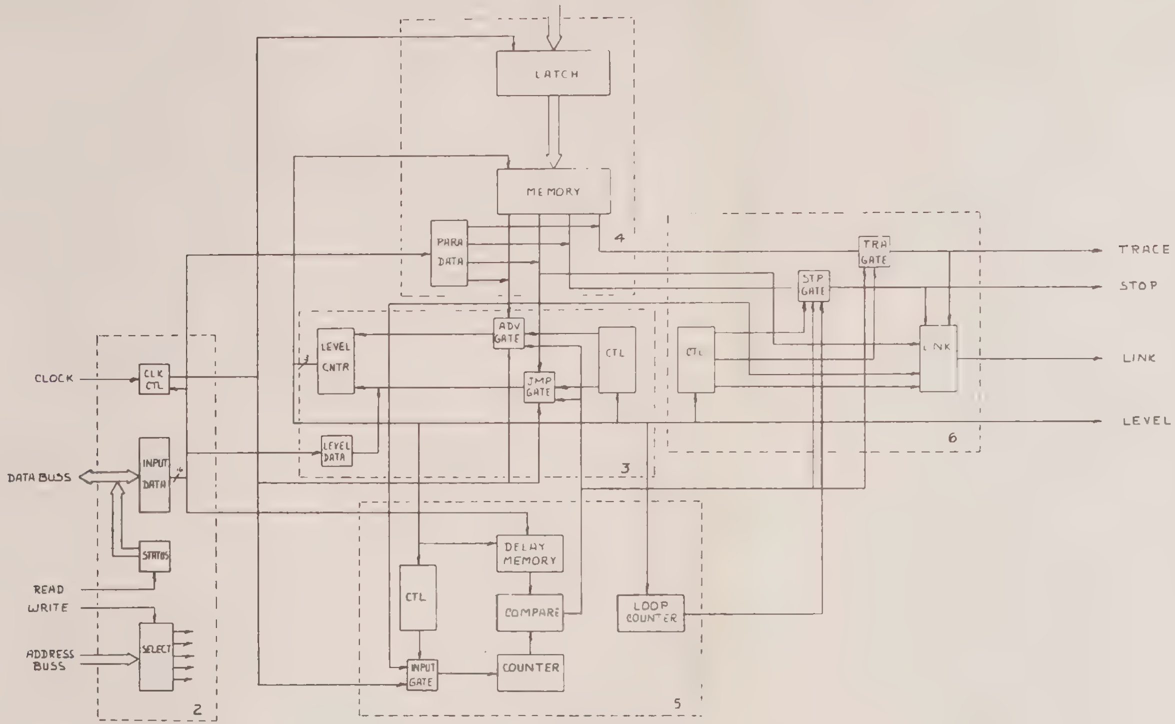
B 0117-0060 REV 62

MODEL K105 SHEET 2 OF 2

KLINGLER K-VEL M10

0117-0061 | 1 | 62

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 349	RM		
	56	4291	REV'D PER ECO Nº			
	57	4420	REV'D PER ECO	RR		
	58R	4462	REWORK ONLY	MW		
	59R	4477	REWORK ONLY	MW		
	60	4497	REWORK ONLY	MW		
	61	4543	PER ECO			
	62	4563	REVISED PER ECO 4563A	RTM		



NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V, ±20%
[3] COMPONENTS INDICATED ARE USED ON -10 ASSY ONLY.
4. [symbol] OR [symbol] EQUALS SINGLE PULLUP TO +5 (4.7K SIP OR DIP)
5. [symbol] EQUALS TERMINATION +5 3K 6.2K (SIP OR DIP)
6. -□□- BREAK POINT - .120 SQ. PADS SPACED .150 (2:1)

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DASH NO	NUMBER (NEXT ASSEMBLY)	QTY
10	0117-0003	1

DO NOT SCALE DRAWING

TOLERANCE

ENG SERV | DATE

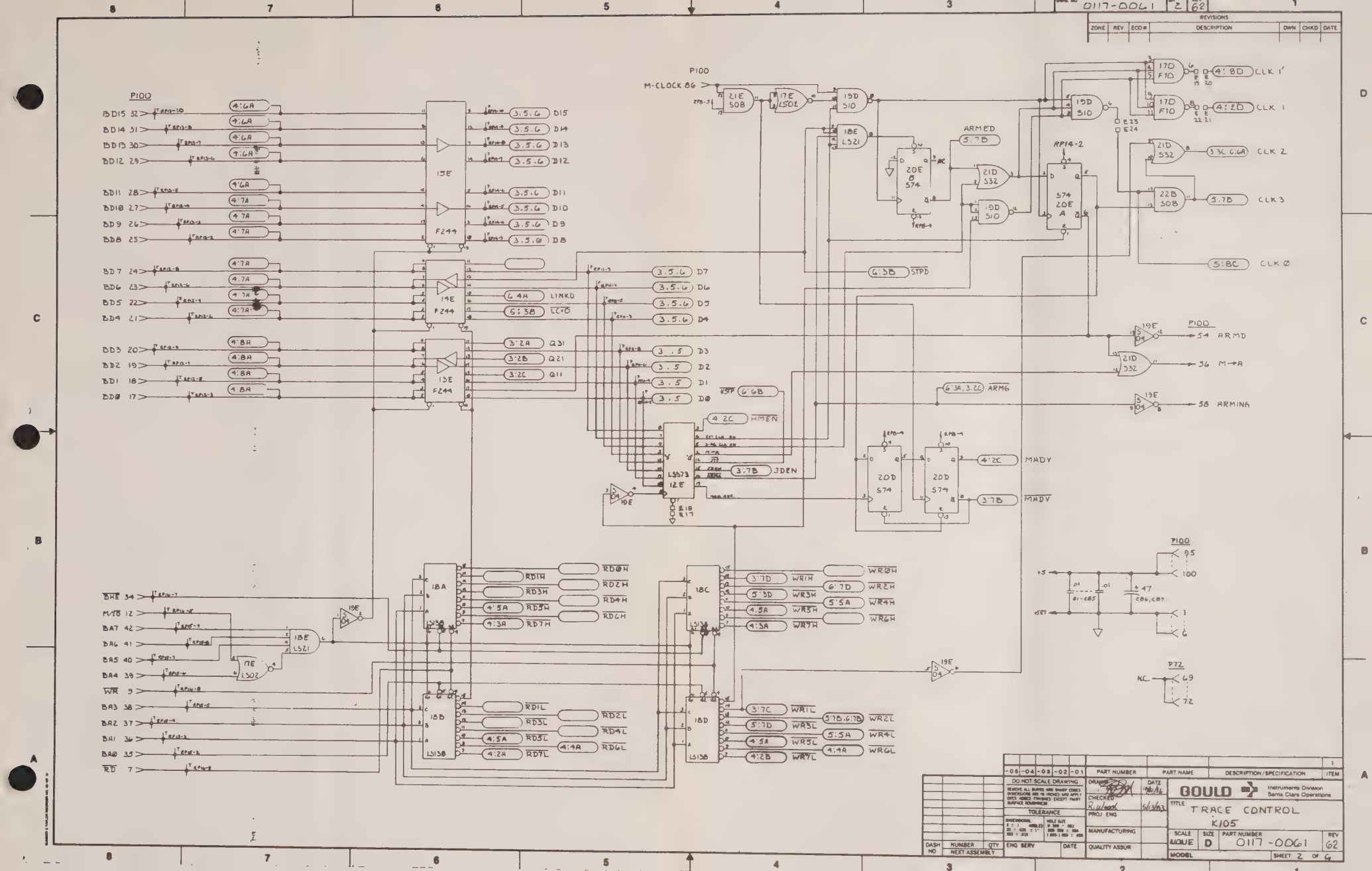
DRAWN — DATE 4/22/80
CHECKED R. Wood — 5/13/83
MANUFACTURING — 5-13-83

GOULD biomation

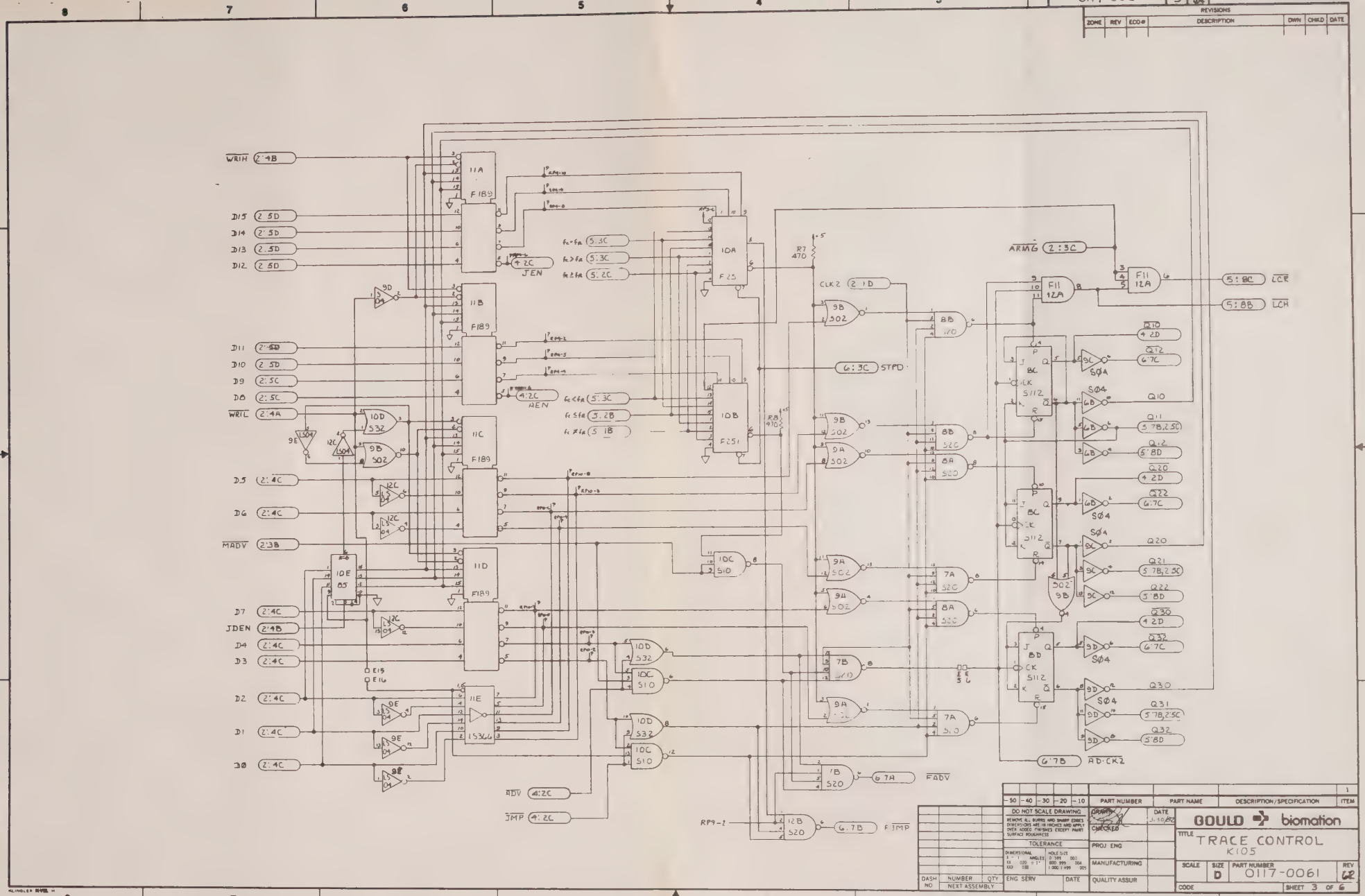
TITLE TRACE CONTROL K105

SCALE	SIZE	PART NUMBER	REV
NONE	D	0117-0061	62

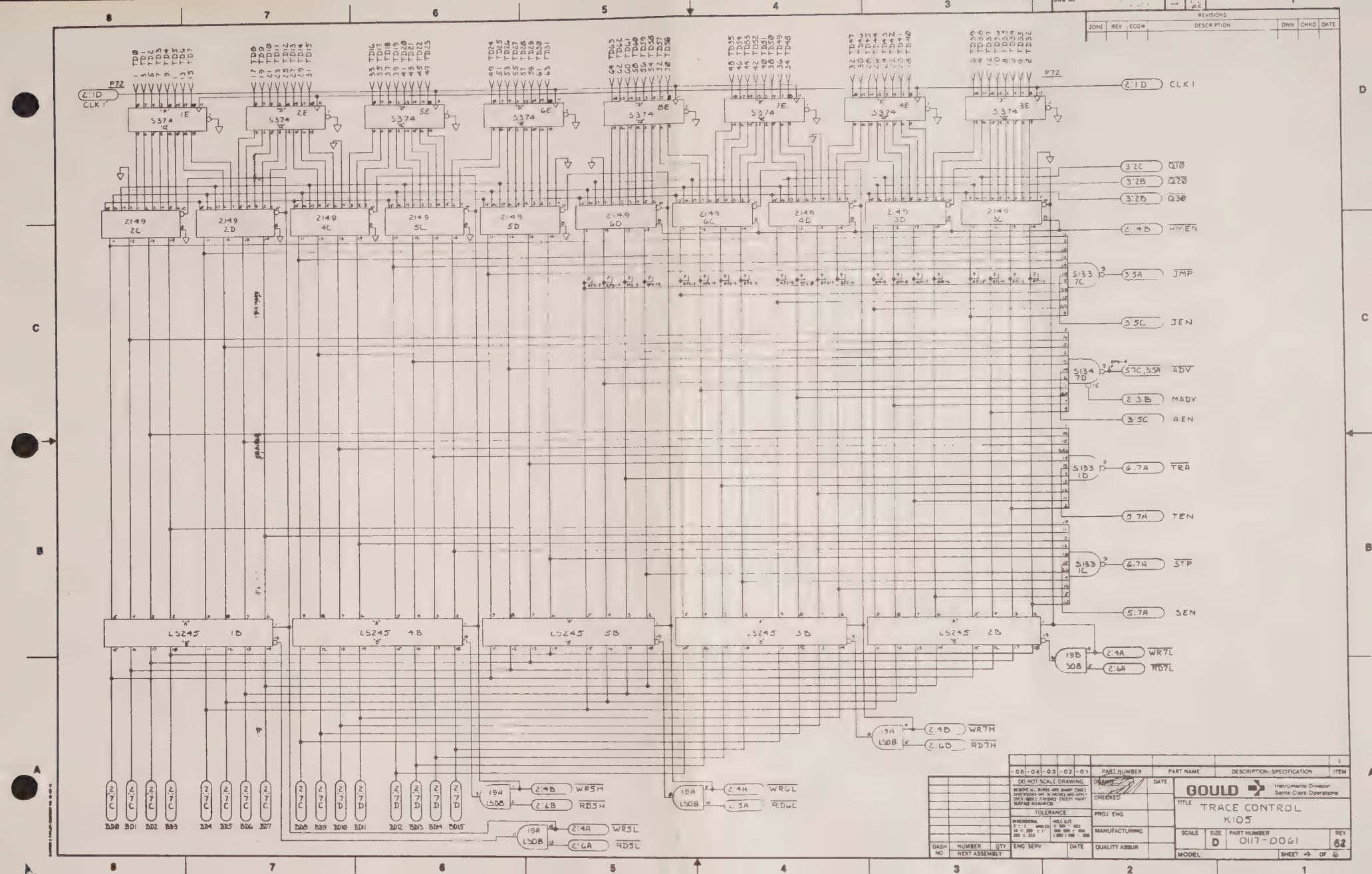
CODE K105 SHEET 1 OF 6

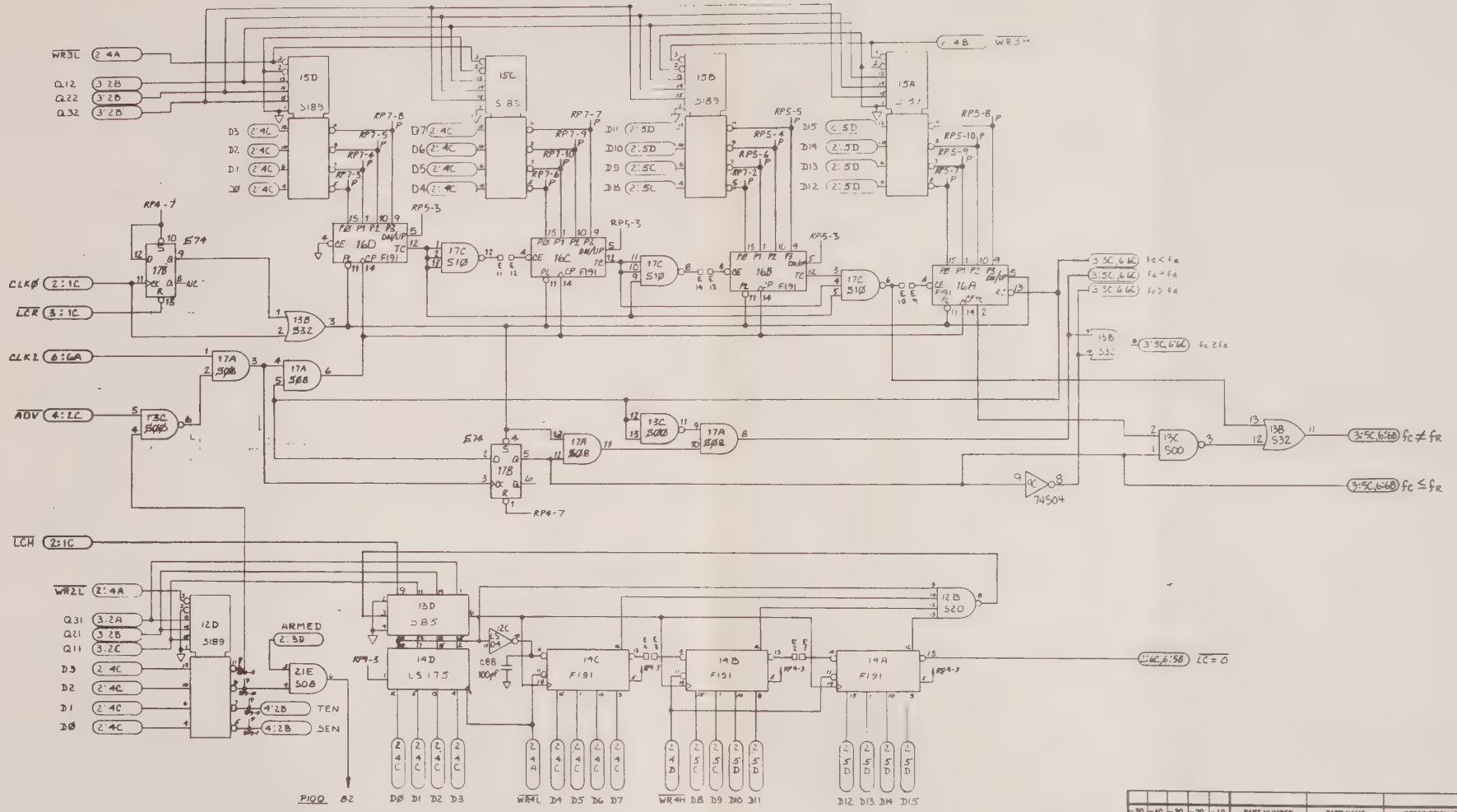


0117-0061
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
P100
BD15 32
BD14 31
BD13 30
BD12 29
BD11 28
BD10 27
BD9 26
BD8 25
BD7 24
BD6 23
BD5 22
BD4 21
BD3 20
BD2 19
BD1 18
BD0 17
BHE 34
M/IO 12
BA7 42
BA6 41
BA5 40
BA4 39
WR 9
BA3 38
BA2 37
BA1 36
BA0 35
RD 7
15E F244
14E F244
13E F244
18A LS138
18B LS138
18C LS138
18D LS138
18E LS21
17E LS02
19E S04
LS373 12E
M-CLOCK 86
21E S08
17E LS02
19D S10
18E LS21
20E S74
21D S32
19D S10
S74 20E A
17D F10
22B S08
21D S32
20D S74
20D S74
LINKD
LC-0
Q31
Q21
Q11
STPD
HMEN
JDEN
ARMED
ARMG
MADV
CLK 1'
CLK 1
CLK 2
CLK 3
CLK 0
ARMD
M→A
ARMING
P72
NC
+5
+SET
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD
Instruments Division
Santa Clara Operations
TITLE
TRACE CONTROL
K105
SCALE
NONE
SIZE
D
PART NUMBER
0117-0061
REV
62
MODEL
SHEET 2 OF 6



REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
WRIH 2:4B
D15 2:5D
D14 2:5D
D13 2:5D
D12 2:5D
D11 2:5D
D10 2:5D
D9 2:5C
D8 2:5C
WRIL 2:4A
D5 2:4C
D6 2:4C
MADV 2:3B
D7 2:4C
JDEN 2:4B
D4 2:4C
D3 2:4C
D2 2:4C
D1 2:4C
D0 2:4C
11A F189
11B F189
11C F189
11D F189
11E LS366
10A F25
10B F251
10C S10
10D S32
10E 85
JEN
AEN
ADV 4:2C
JMP 4:2C
CLK2 2:1D
6:3C STPD
ARMG 2:3C
F11 12A
5:8C LCR
5:8B LCH
Q10 4:2D
Q12 6:7C
Q11 5:7B,2:5C
Q12 5:8D
Q20 4:2D
Q22 6:7C
Q21 5:7B,2:5C
Q22 5:8D
Q30 4:2D
Q32 6:7C
Q31 5:7B,2:5C
Q32 5:8D
6:7B AD·CK2
6:7A FADV
6:7B FJMP
RP9-2
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE TRACE CONTROL K105
SCALE
SIZE D
PART NUMBER 0117-0061
REV 62
SHEET 3 OF 6
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE
PROJ ENG
MANUFACTURING
QUALITY ASSUR
CHECKED


REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
P72
2:1D CLK1
S374 1E
S374 2E
S374 3E
S374 4E
S374 5E
S374 6E
S374 7E
S374 8E
2149 2C
2149 2D
2149 4C
2149 5C
2149 5D
2149 6D
2149 6C
2149 4D
2149 3D
2149 3C
S133 7C
S134 7D
S133 1D
S133 1C
LS245 1B
LS245 4B
LS245 5B
LS245 3B
LS245 2B
19B LS08
19A LS08
CLK1
3:2C Q1Ø
3:2B Q2Ø
3:2D Q3Ø
2:4B HMEN
3:5A JMP
3:5C JEN
57C,35A ADV
2:3B MADY
3:5C AEN
6:7A TRA
5:7A TEN
6:7A STP
5:7A SEN
2:4A WR7L
2:6A RD7L
2:4B WR7H
2:6D RD7H
2:4B WR5H
2:6B RD5H
2:4A WR5L
2:6A RD5L
2:4A WR6L
2:5A RD6L
BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7
BD8 BD9 BD10 BD11 BD12 BD13 BD14 BD15
DO NOT SCALE DRAWING
TOLERANCE
DASH NO | NUMBER | QTY
NEXT ASSEMBLY
ENG SERV | DATE
PART NUMBER | PART NAME | DESCRIPTION: SPECIFICATION | ITEM
DRAWN | DATE
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD Instruments Division Santa Clara Operations
TITLE
TRACE CONTROL
K105
SCALE | SIZE | PART NUMBER | REV
D | 0117-0061 | 62
MODEL
SHEET 4 OF 6



REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

TOLERANCE

	DRAWN	DATE
	CHECKED	
ENG SERV	PROJ ENG	
DATE	MANUFACTURING	
	QUALITY ASSUR	

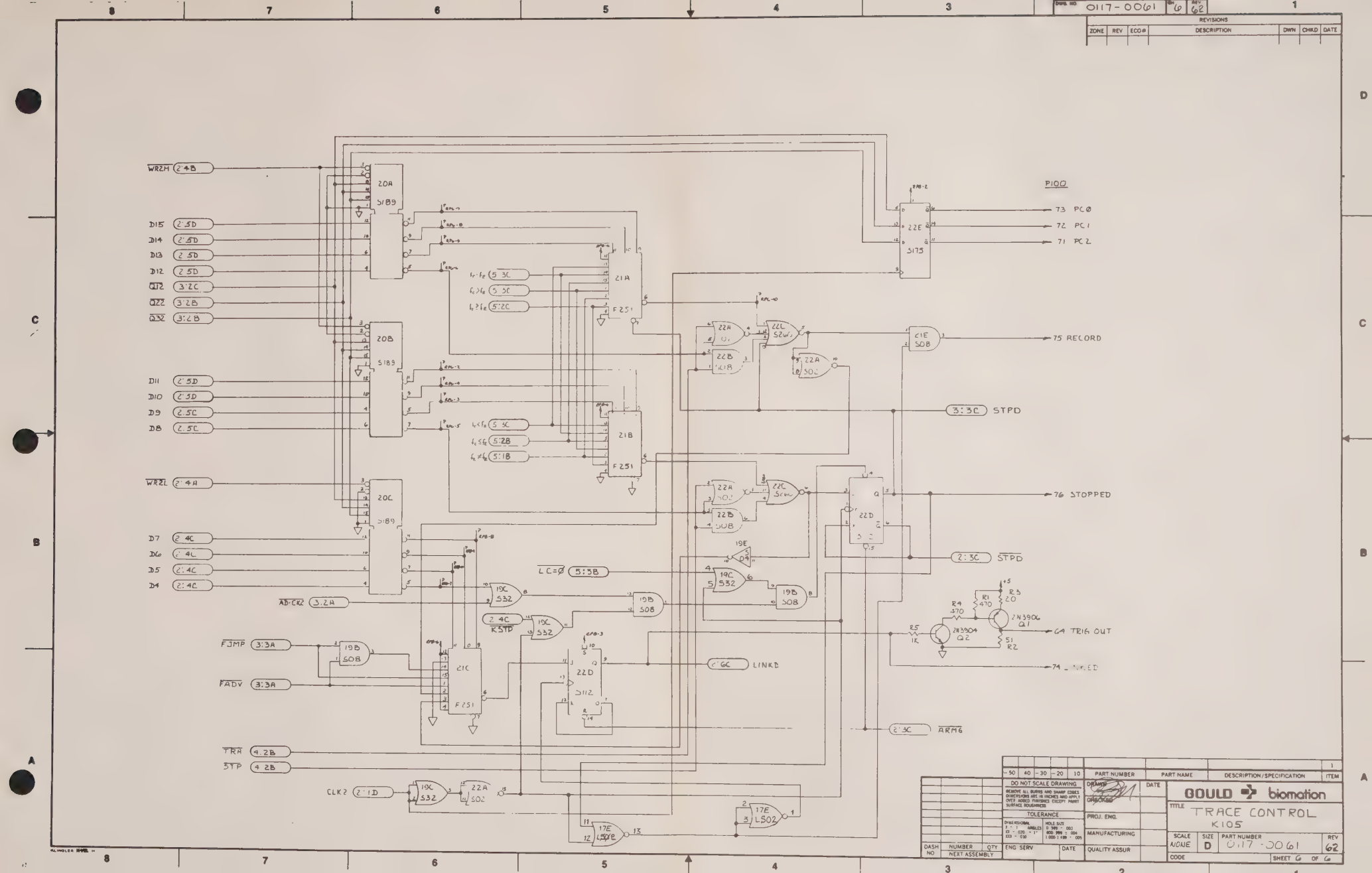
GOULD biomation

TITLE: TRACE CONTROL
K105

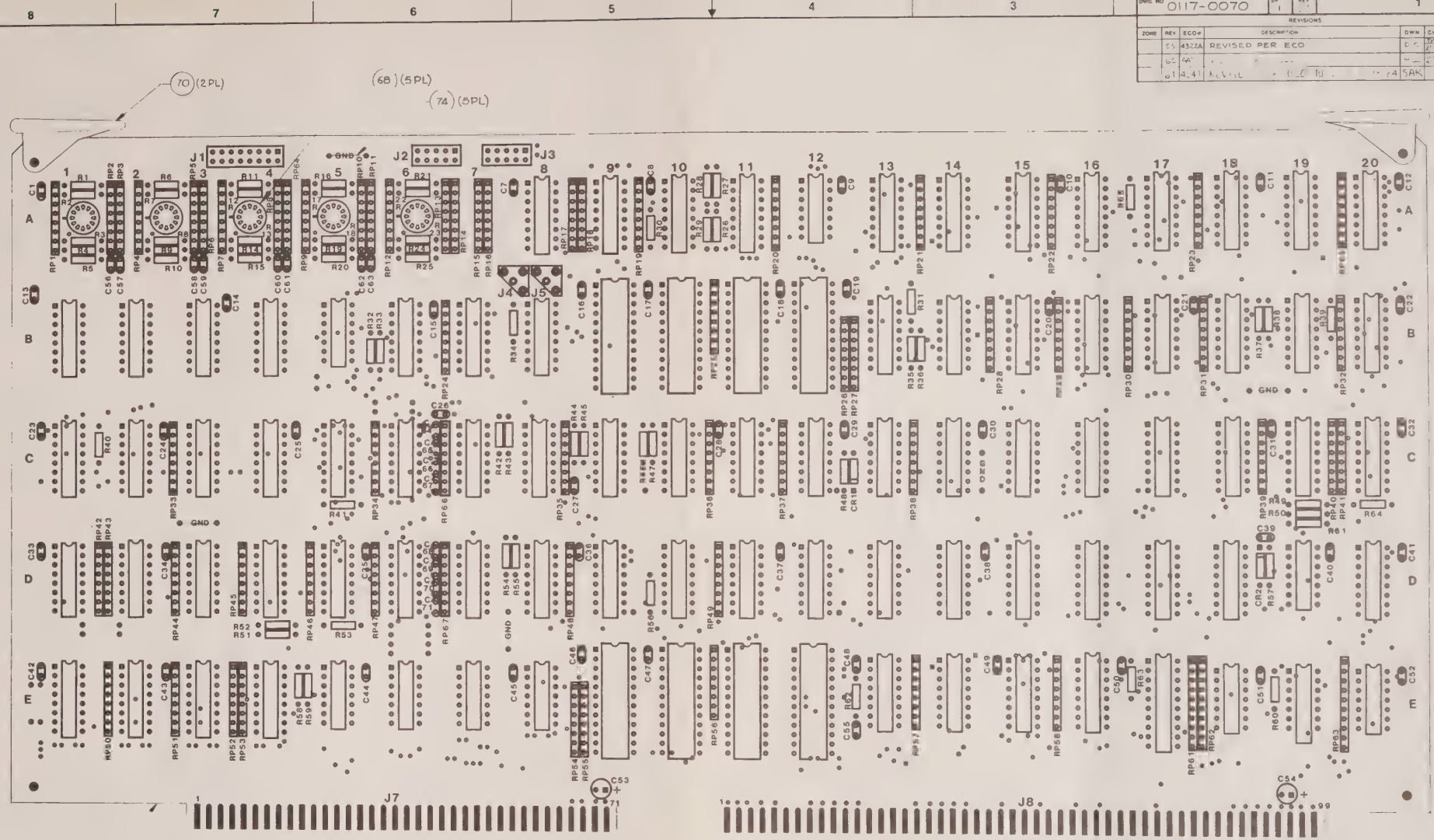
SCALE	SIZE	PART NUMBER	REV
	D	0117-0061	G2

CODE

SHEET 5 OF 6



0117-0061
6
62
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
WR2H 2:4B
D15 2:5D
D14 2:5D
D13 2:5D
D12 2:5D
Q12 3:2C
Q22 3:2B
Q32 3:2B
D11 2:5D
D10 2:5D
D9 2:5C
D8 2:5C
WR2L 2:4A
D7 2:4C
D6 2:4C
D5 2:4C
D4 2:4C
AD-CK2 3:2A
FJMP 3:3A
FADV 3:3A
TRA 4:2B
STP 4:2B
CLK2 2:1D
20A S189
20B S189
20C S189
21A F251
21B F251
21C F251
22A S02
22B S08
22C S260
22D S112
22E S175
21E S08
19C S32
19B S08
19E S04
17E LS02
P100
73 PC0
72 PC1
71 PC2
75 RECORD
3:3C STPD
76 STOPPED
2:3C STPD
64 TRIG OUT
74 LINKED
2:3C ARMG
LC=0 5:3B
2:4C KSTP
2:6C LINKD
R1 470
R3 20
R4 470
R5 1K
2N3904 Q2
2N3906 Q1
S1 R2
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
TRACE CONTROL
K105
SCALE NONE
SIZE D
PART NUMBER 0117-0061
REV 62
CODE
SHEET 6 OF 6



DWG NO	REV
0117-0070	

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	51	4322A	REVISED PER ECO			
	62	44				
	61	4.41			SAK	

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

MATERIAL

FINISH

GOULD PART NO

APPROVALS	DATE
DRAWN	
CHECKED	
PROJ ENG	

DO NOT SCALE DRAWING

DASH NO	NEXT ASSY	USED ON
FIRST APPLICATION		

GOULD
ELECTRONICS

TITLE ASSEMBLY
HIGH SPEED TIMING BD

SIZE	DWG NO	REV
D	0117-0070	

SCALE MODEL SHEET 1 OF 1

GOULD

TITLE			DRAWING NO.	REV
ASSEMBLY HIGH SPEED TIMING BD.	LM		0117-0070	61
DWN D.C. / CHK / ENG / MFG	MODEL K105		SHEET 1 OF 4	

ITEM NO.	PART NUMBER	QTY PER ASSY -10	-20	-30	-40	-50	U/M	DESCRIPTION	REFERENCE DESIGNATION
1	0117-0072	1						FABRICATION	
2									
3									
4									
5									
6									
7	1850-0131-10	1						I.C. MC10H016	19C
8	1700-0008	5						CA3049T	1A,2A,4A-6A
9	1800-0107	3						74LS04	12A,5B,18E
10	1800-0571	2						74LS09	5E,7E
11	1800-0123	1						74LS14	20E
12	1800-0111	1						74LS20N	19D
13	1800-0365	2						74LS28	6E,8E
14	1800-0117	1						74LS86	19E
15	1800-0193	1						74LS138	20D
16	1800-0240-10	1						I.C. 74LS244N	17E

REV	ECO	CHK	APPD	DATE
59	4322A	DGW		2/4/
60	4417	DGW		4/
61	4641			

NOTES:

DASH #	NEXT ASSY	QTY
10	0117-0800-10	1
10	0117-0810-10	1

GOULD

TITLE		DRAWING NO.	REV
ASSEMBLY HIGH SPEED TIMING BD.	LM	0117-0070	61
	MODEL K105	SHEET 2 OF 4	

ITEM NO.	PART NUMBER	QTY PER ASSY -10	-20	-30	-40	-50	U/M	DESCRIPTION	REFERENCE DESIGNATION
17	1850-0055-10	4						I.C MC 10016	15B,16B,17B,18B
18	1850-0037	4						MC 10101	10C,11C,10D,11D
19	1850-0002	7						MC 10102	11A,13A,5C,6C,20C,5D,6D
20	1850-0049	1						MC 10103	8B
21	1850-0057	1						MC 10104	14D
22	1850-0003	1						MC 10105	14B
23	1850-0025	2						MC 10106	15A,20B
24	1850-0026	1						MC 10109	13C
25	1850-0006	3						MC 10131	16A,19A,13D
26	1850-0083	8						F10136	7C,8C,9C,12C,7D,8D,9D,12D
27	1850-0034	2						MC 10176	6B,20A
28	1850-0035	1						MC 10210	14A
29	1850-0043	5						MC 10216	8A,1B,2B,3B,4B
30	1850-0019	4						MC 10231P	7B,13B,17A,19B
31	1850-0088	8						HM 10422	9B-12B,9E-12E
32	1850-0135	4						MC 10H100	1C-4C
33	1850-0133	1						MC 10H121	9A
34	1850-0119	10						MC 10H131	14C,1D-4D,1E-4E,18A
35	1850-0134	1						MC 10H211	10A
36	1820-0053-10	8						I.C. 4724	15C-18C,15D-18D

GOULD

TITLE ASSEMBLY
HIGH SPEED TIMING BD.

LM

DRAWING NO. 0117-0070

REV 01

MODEL K105

SHEET 3 OF 4

ITEM NO.	PART NUMBER	QTY PER ASSY -10	-20	-30	-40	-50	U/M	DESCRIPTION	REFERENCE DESIGNATION
37	1800-0555-10	4						IC MC3486	13E-16E
38	3000-8206	12						RESISTOR, 82Ω ¼W, 5% CAR	R27,28,33,35,37,42,45,47,50,51,54,58
39	3000-9106	10						91Ω	R1,4,6,9,11,14,16,19,21,24
40	3000-1100	5						110Ω	R5,10,15,20,25
41	3000-1300	12						130Ω	R26,29,32,36,38,43,44,46,49,52,55,59
42	3000-3300	4						330Ω	R30,56,61,62
43	3000-5100							510Ω	R2,3,7,8,12,13,17,18,22,23,31,39,65,66
44	3000-4701	5						4.7K	R40,41,48,53,60
45	3000-2001							2K	R57,63,67,68
46	3000-7500	1						RESISTOR, 750, ¼W, 5% CAR	R64
47	3700-0046	1						RES. PACK, 270, .2W, 2%, 8PIN	RP17
48	3700-0102	1						150Ω	RP18
49									
50	3700-0069	2						2K	RP57,58
51	3700-0123	5						430, .2W, 2%, 8PIN	RP1,4,7,9,12
52	3700-0031	28						330, .3W, 2%, 8PIN	RP65,13,15,21-28,33,35-38,
53		–							41-46,48,49,52,54,55,56
54	3700-0041	11						4.7K, .2W, 2%, 8PIN	RP19,20,29-32,34,39,40,47,53
55	3700-0049	3						3K/6.2K, ⅛W, 5%, 10P	RP61-63
56	3700-0021-10	4						RES PACK 470Ω .3W, 2%, 8PIN	RP2,5,8,10

GOULD

TITLE ASSEMBLY
HIGH SPEED TIMING BD.

LM

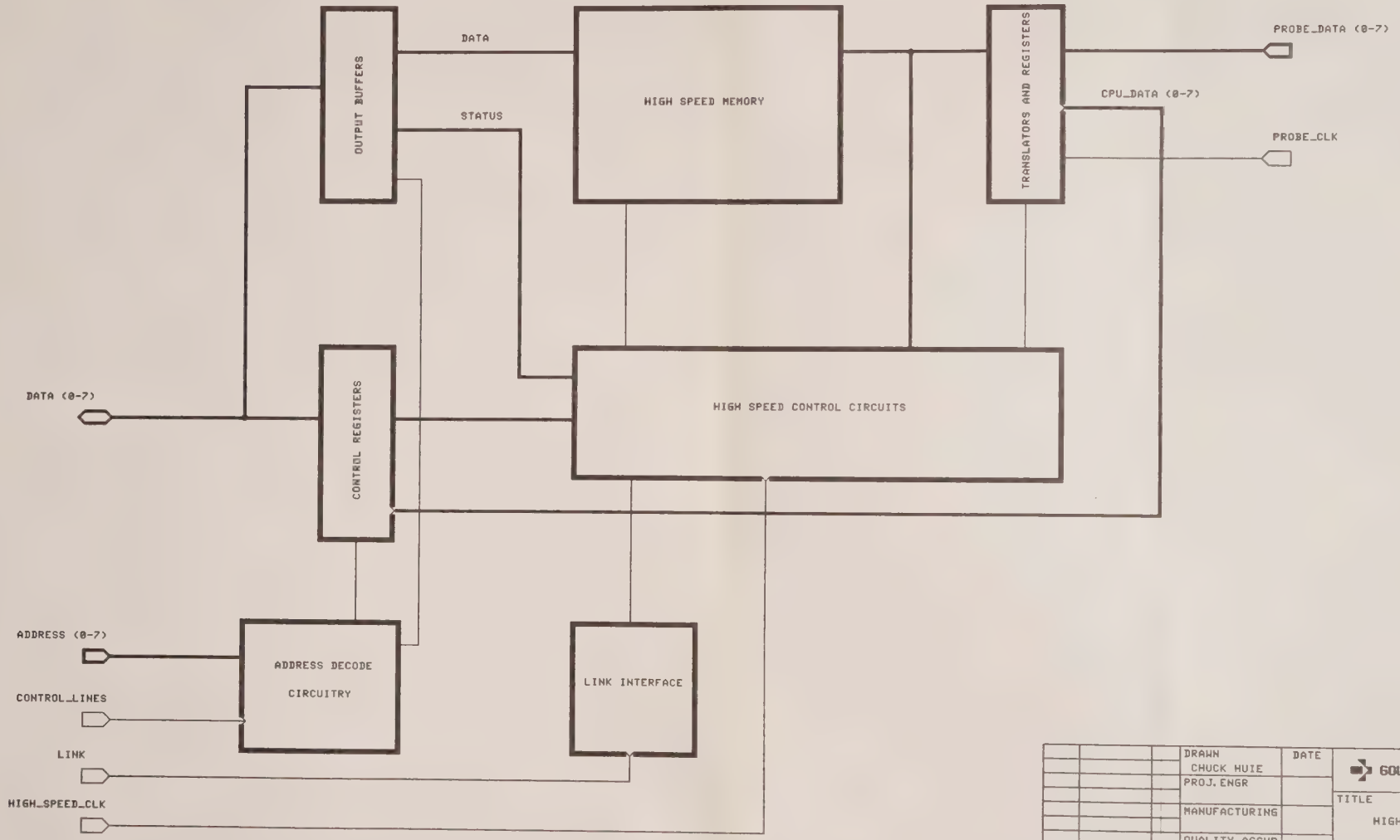
DRAWING NO. 0117-0070

REV 01

MODEL K105

SHEET 4 OF 4

ITEM NO.	PART NUMBER	QTY PER ASSY -10	-20	-30	-40	-50	U/M	DESCRIPTION	REFERENCE DESIGNATION
57	3000-4700-10	1						RESISTOR 470, ¼W, 5%, CAR	R34
58	3700-0016	2						RES PACK, 1K, ⅛W, 2%, 8PIN	RP50,51
59	3700-0117	4						RES PACK 68Ω .3W, 2% 8PIN	RP3,6,11,64
60	6000-0438-10	1						CONN. HDR., 16PIN, STR, D.ROW	J1
61	6000-0438-20	2						CONN. HDR 10PIN. STR D ROW	J2,3
62	6000-0555-10	2						COAX. CONN.	J4,5
63	6000-0557	2						SOCKET, COAX. CONN.	J4,5
64	1000-0002	2						DIODE 1N4152	CR1,2
65	4000-0025	1						CAPACITOR .1uf, 50V, 20%	C39
66	4010-0103	63						CAPACITOR .01uf, 50V, 10%	C1,7-38,40-52,55-71
67	4400-0043	2						CAPACITOR 47uf 6V	C53,54
68	7000-0381	5						MOUNTING PADS	1A,2A,4A,5A,6A
69	7000-0412	2						CARD EJECTOR PIN	
70	7000-0120	2						CARD EJECTOR	
71	3700-0019	2						RES PACK 220Ω, .3W, 2%, 8PIN	RP14,16
72	0117-0155-10	1						JUMPER CABLE ASSY.	
73									
74	9000-0094	5						BUSS WIRE FORMED	GND
75									
76	3700-0110-10	2						RES PACK 100Ω .3W, 5%	RP66,67



			DRAWN CHUCK HUIE	DATE
			PROJ. ENGR	
			MANUFACTURING	
			QUALITY ASSUR	
DASH NO.	NUMBER NEXT ASSEMBLY	QTY	ECO NO.	

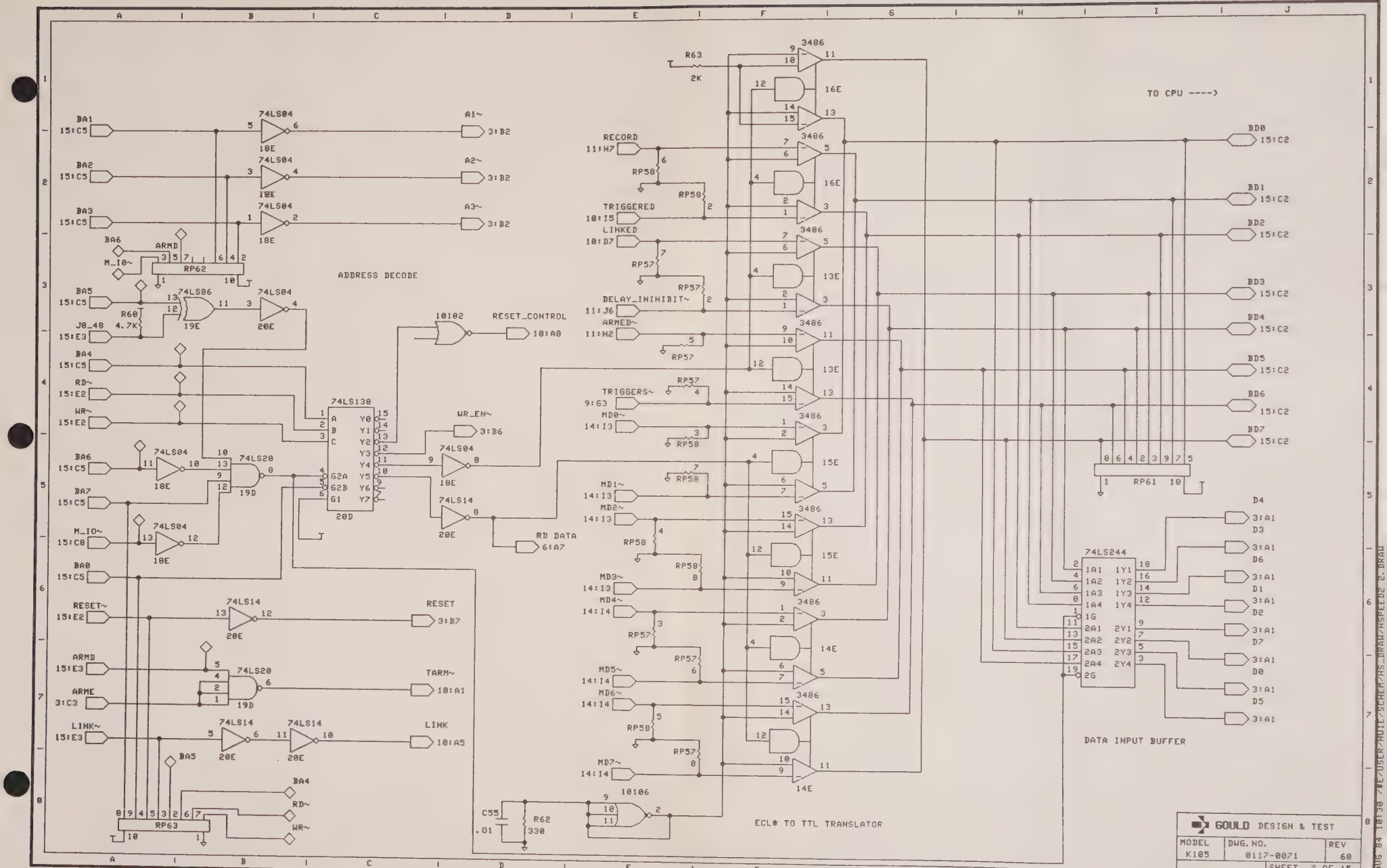
GOULD DESIGN & TEST

TITLE
HIGH SPEED TIMING BD

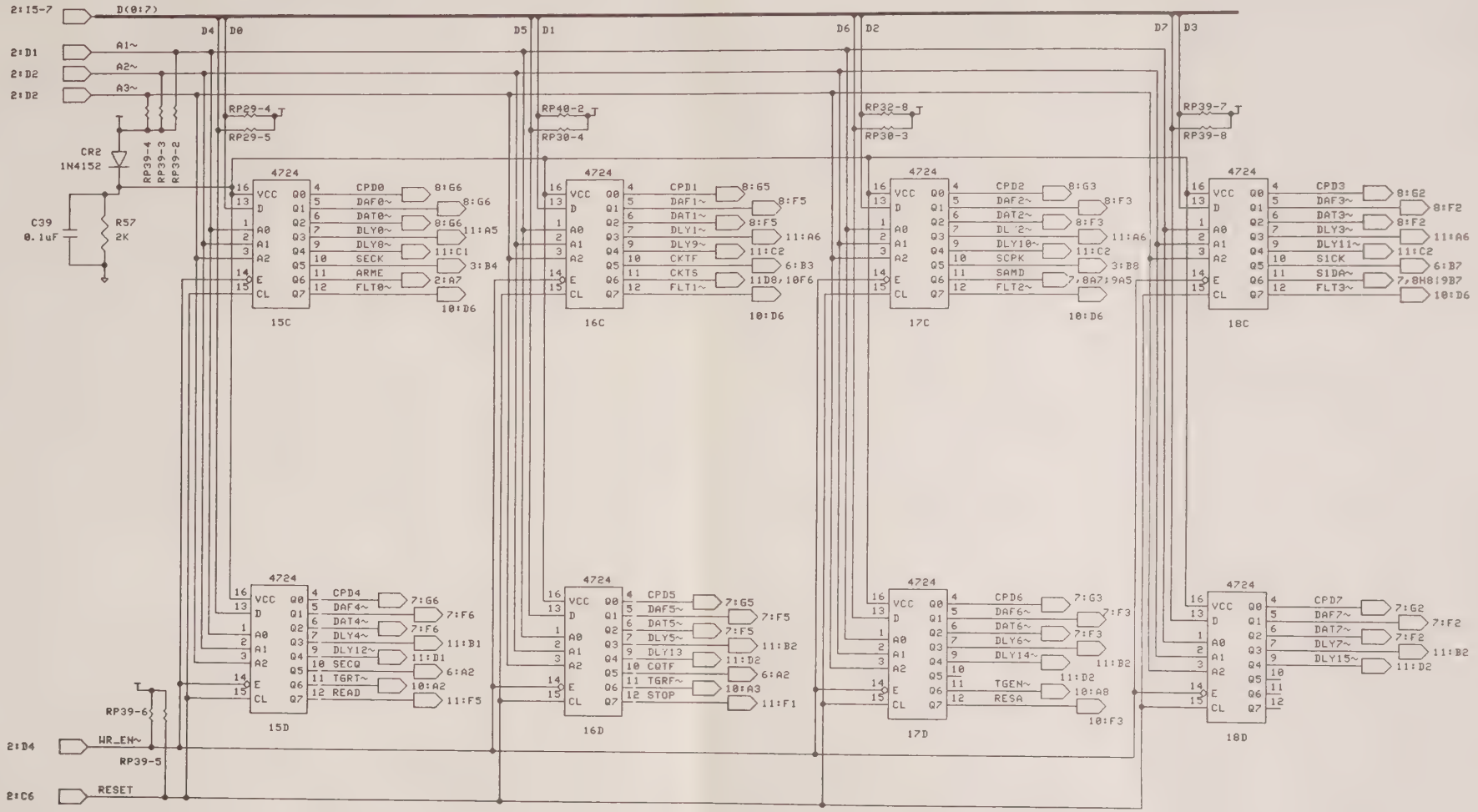
MODEL	PART NUMBER	REV
K105	0117-0071	60

SHEET 1 OF 15

AUG 84 12:04 */E/USER/HUIE/SCHEM/HS_DRAW/HSPEED2 1.DRAW



ADDRESS DECODE
ECL* TO TTL TRANSLATOR
DATA INPUT BUFFER
TO CPU ---->
74LS138
74LS244
74LS04
74LS86
74LS20
74LS14
3486
10102
10106
RESET_CONTROL
WR_EN~
RD DATA
RESET
TARM~
LINK
RECORD
TRIGGERED
LINKED
DELAY_INIHIBIT~
ARMED~
TRIGGERS~
MD0~
MD1~
MD2~
MD3~
MD4~
MD5~
MD6~
MD7~
RP62
RP63
RP61
RP58
RP57
R63
2K
R60
4.7K
R62
330
C55
.01
GOULD DESIGN & TEST
MODEL K105
DWG. NO. 0117-0071
REV 60

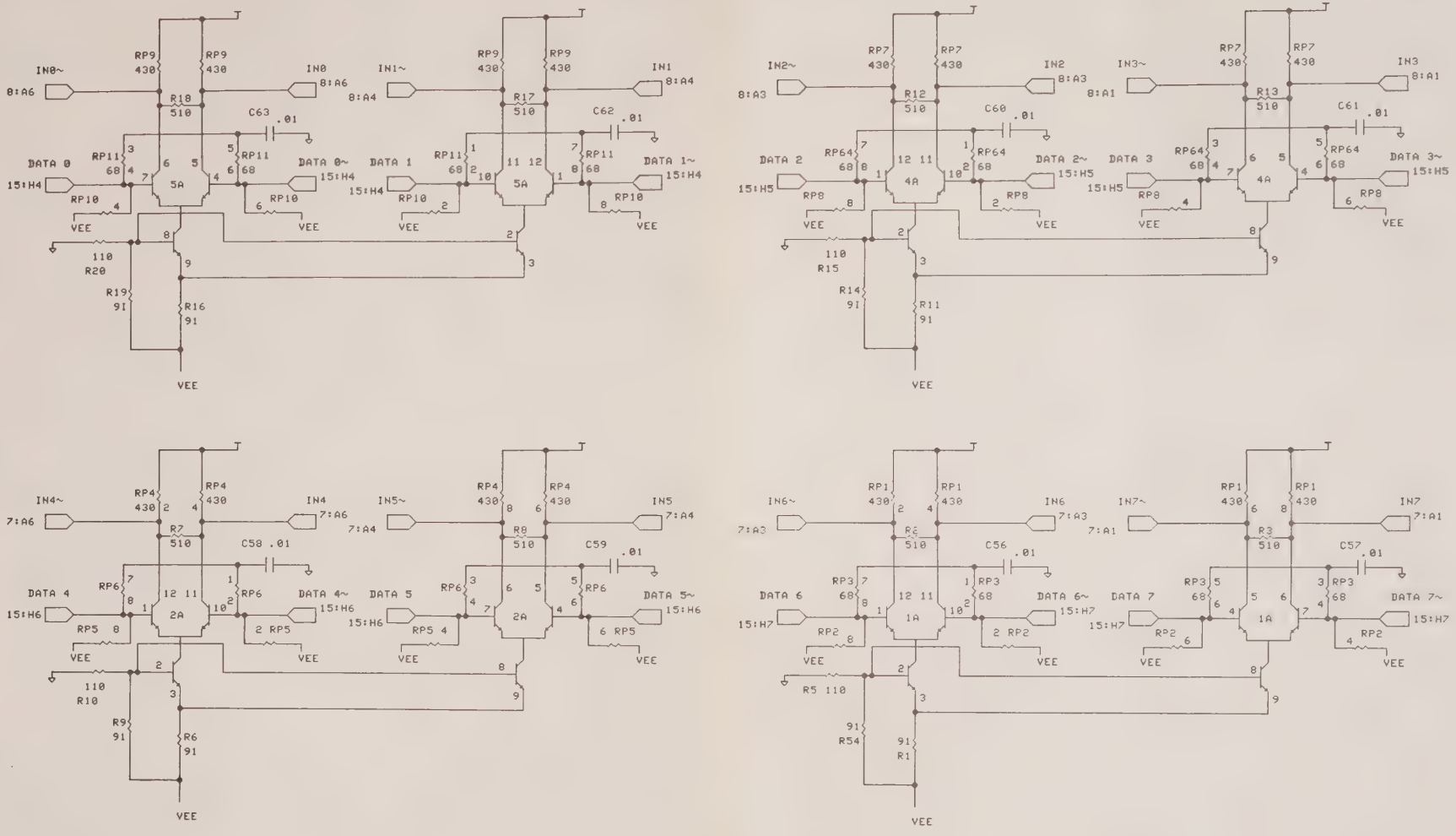


CONTROL LATCHES

GOULD DESIGN & TEST

MODEL	DWG. NO.	REV
K105	0117-0071	60

SHEET 3 OF 15



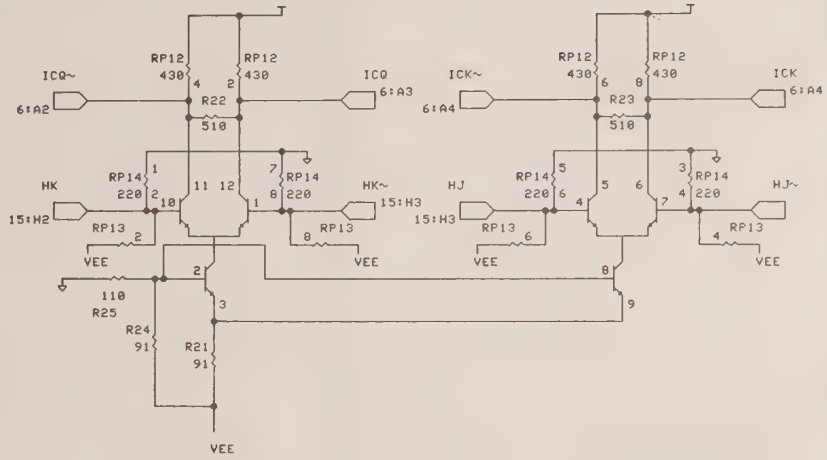
ECL TO ECL# TRANSLATORS

GOULD DESIGN & TEST

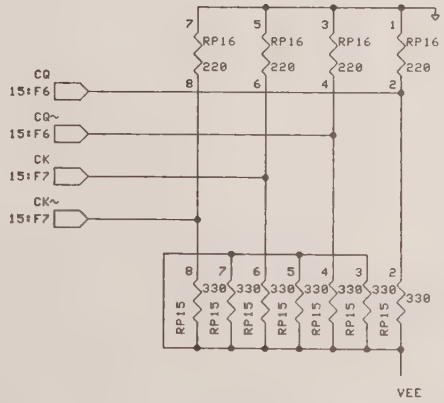
MODEL	DWG. NO.	REV
K105	0117-0071	60

SHEET 4 OF 15

2 AUG 84 10:35 /$E/USER/HUIE/SCHEM/HS_DRAW/HSPEED2 4.DRAW

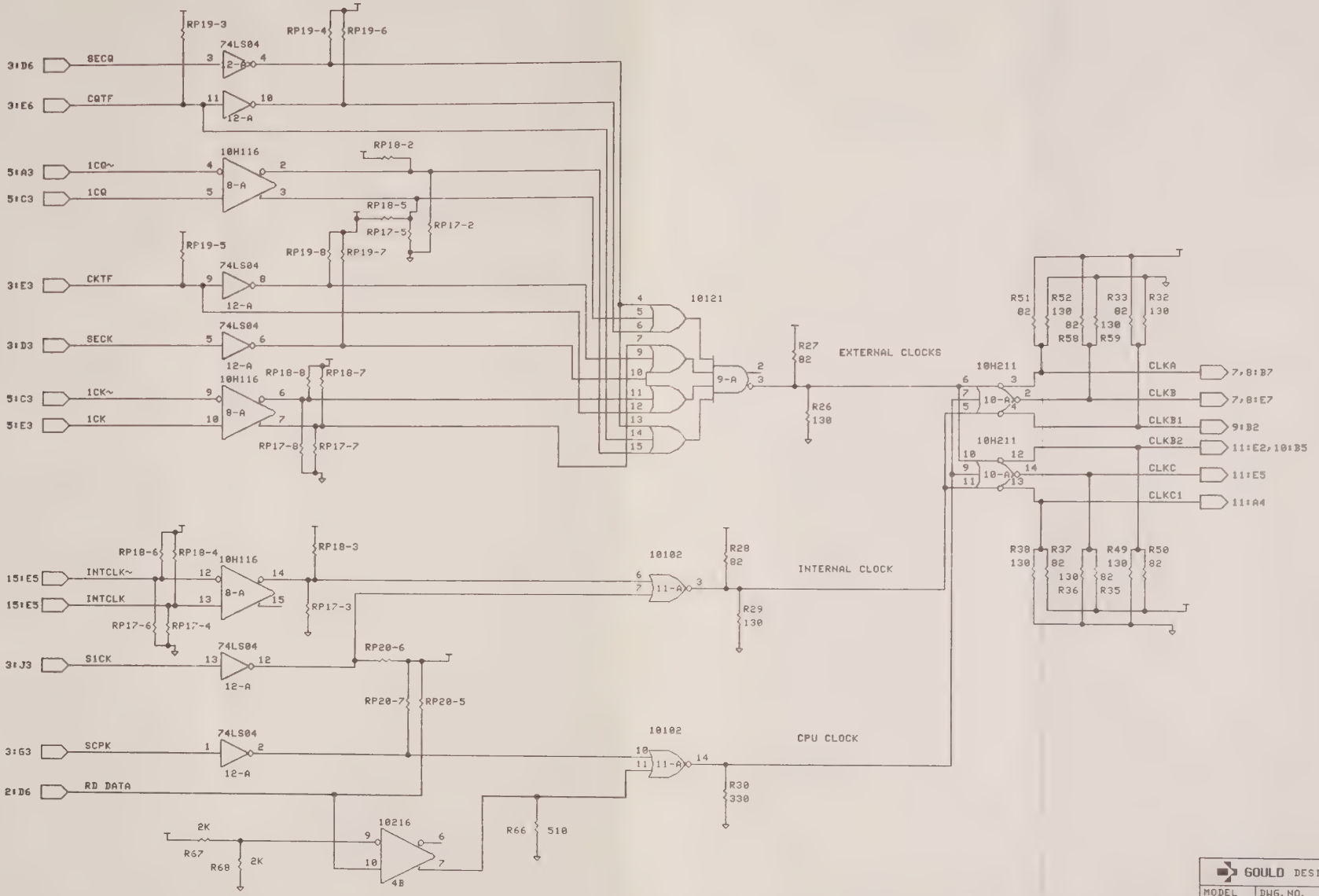


ECL TO ECL* TRANSLATORS FOR CLKS



DUMMY LOADS

GOULD DESIGN & TEST		
MODEL K105	DWG. NO. 0117-0071	REV 60
	SHEET 5 OF 15	

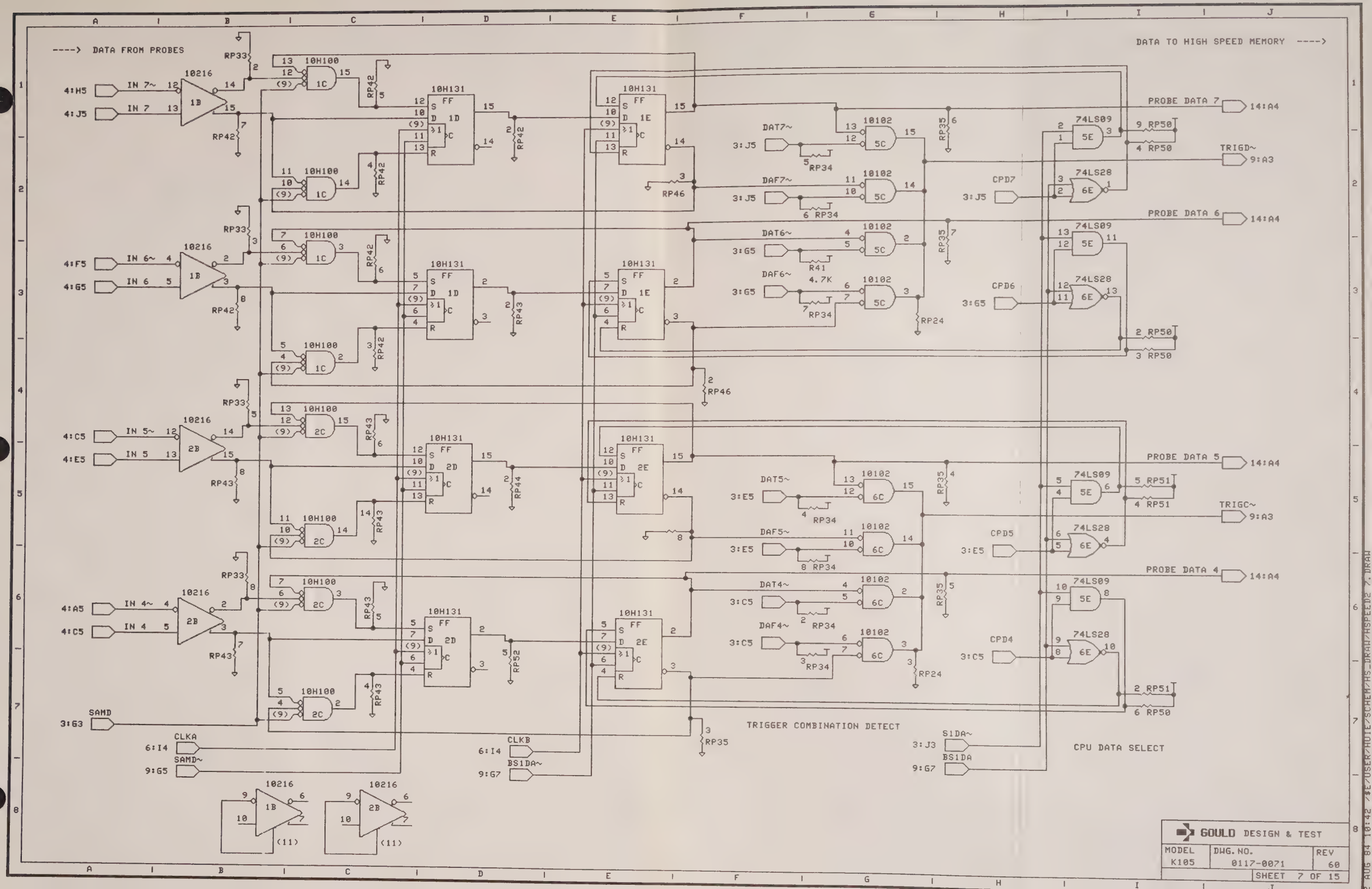


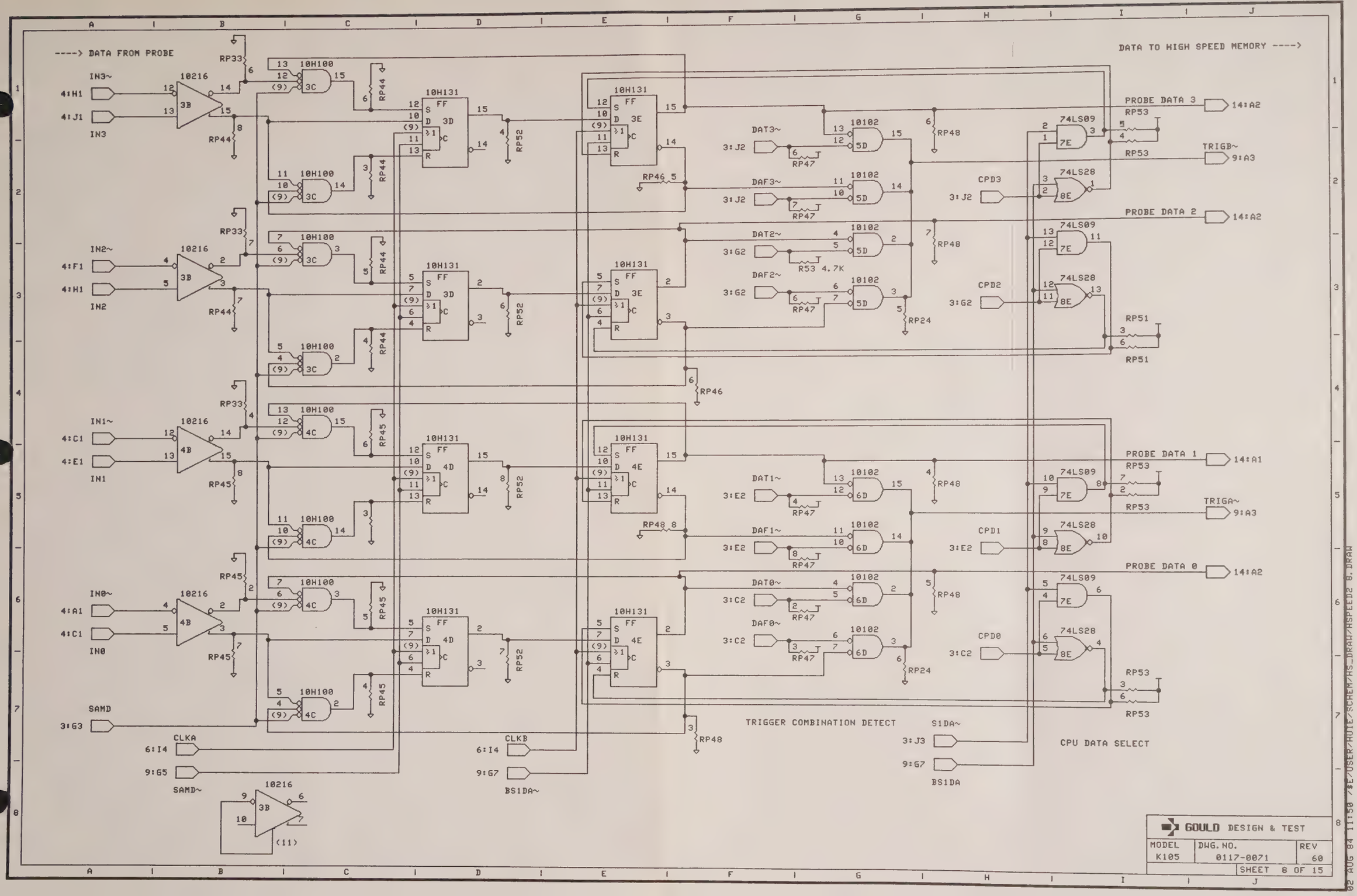
GOULD DESIGN & TEST

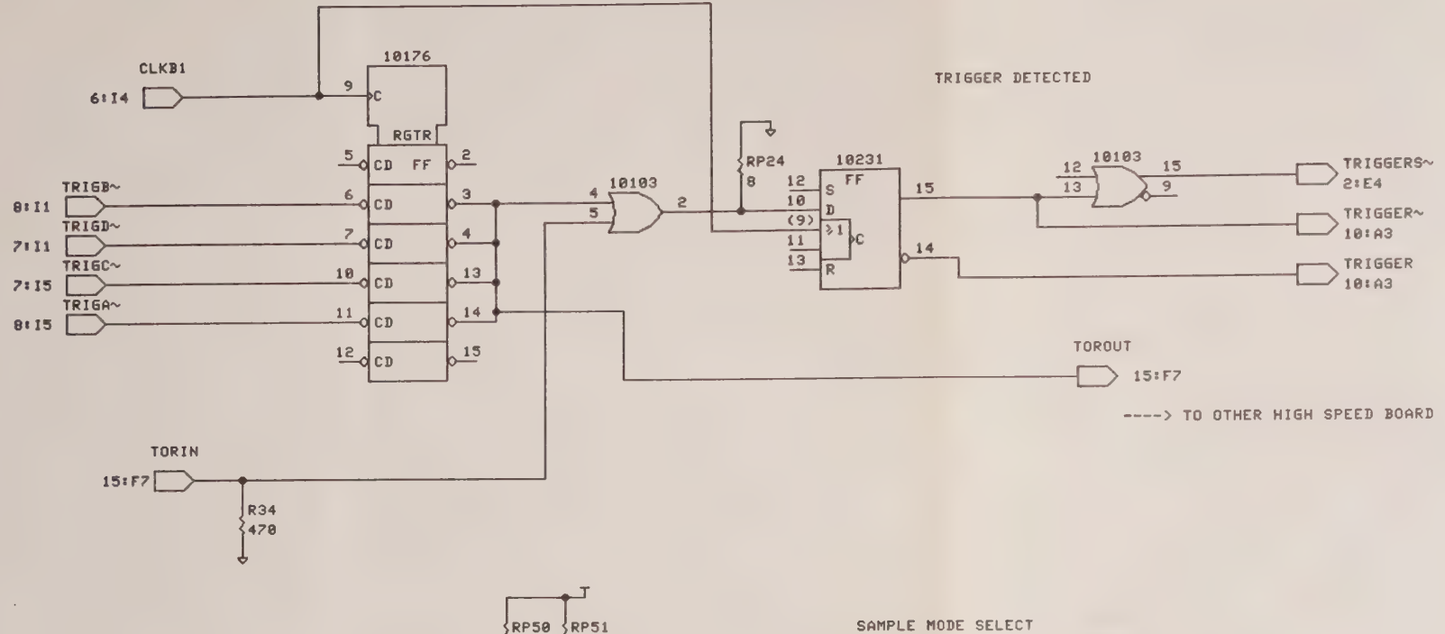
MODEL	DWG. NO.	REV
K105	0117-0071	60

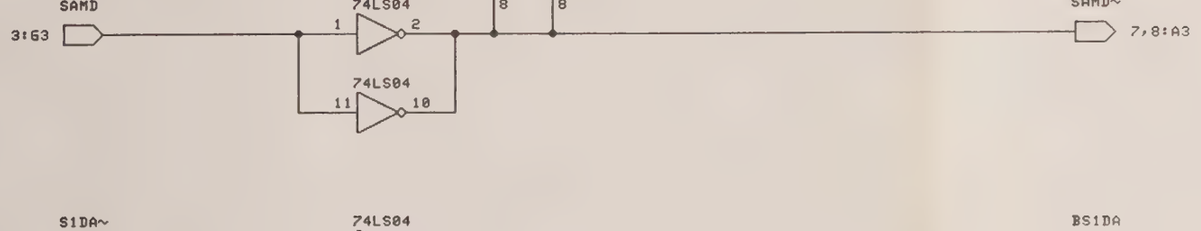
SHEET 6 OF 15

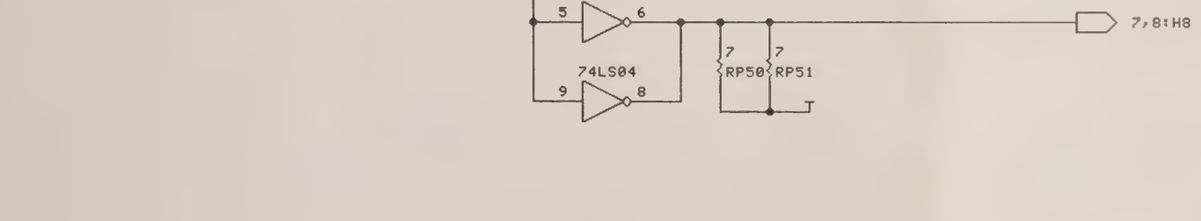
AUG 84 10:39 */E2/USER/HUTF/SCHEM/HS_DRAW/HSPED2 6.DRAW


----> DATA FROM PROBES
DATA TO HIGH SPEED MEMORY ---->
4:H5
4:J5
4:F5
4:G5
4:C5
4:E5
4:A5
4:C5
3:G3
SAMD
6:I4
CLKA
SAMD~
9:G5
6:I4
CLKB
BS1DA~
9:G7
3:J5
3:G5
3:E5
3:C5
3:J5
3:J3
BS1DA
9:G7
10216
10H100
10H131
10102
74LS09
74LS28
RP33
RP42
RP43
RP44
RP46
RP24
RP34
RP35
RP50
RP51
R41
4.7K
PROBE DATA 7
PROBE DATA 6
PROBE DATA 5
PROBE DATA 4
TRIGD~
TRIGC~
CPD7
CPD6
CPD5
CPD4
TRIGGER COMBINATION DETECT
CPU DATA SELECT
GOULD DESIGN & TEST
MODEL K105
DWG. NO. 0117-0071
REV 60
SHEET 7 OF 15
AUG 84 10:42 /$E/USER/HUIE/SCHEM/HS_DRAW/HSPEED2_7.DRAW


----> DATA FROM PROBE
DATA TO HIGH SPEED MEMORY ---->
IN3~
4:H1
4:J1
IN3
IN2~
4:F1
4:H1
IN2
IN1~
4:C1
4:E1
IN1
IN0~
4:A1
4:C1
IN0
SAMD
3:G3
CLKA
6:I4
9:G5
SAMD~
CLKB
6:I4
9:G7
BS1DA~
S1DA~
3:J3
9:G7
BS1DA
10216
3B
4B
10H100
3C
4C
10H131
FF
3D
4D
3E
4E
RP33
RP44
RP45
RP52
RP46
RP47
RP48
RP53
RP51
RP24
R53 4.7K
10102
5D
6D
74LS09
7E
74LS28
8E
DAT3~
3:J2
DAF3~
3:J2
DAT2~
3:G2
DAF2~
3:G2
DAT1~
3:E2
DAF1~
3:E2
DAT0~
3:C2
DAF0~
3:C2
CPD3
3:J2
CPD2
3:G2
CPD1
3:E2
CPD0
3:C2
PROBE DATA 3
14:A2
PROBE DATA 2
14:A2
PROBE DATA 1
14:A1
PROBE DATA 0
14:A2
TRIGB~
9:A3
TRIGA~
9:A3
TRIGGER COMBINATION DETECT
CPU DATA SELECT
GOULD DESIGN & TEST
MODEL K105
DWG. NO. 0117-0071
REV 60
SHEET 8 OF 15
02 AUG 84 11:50 /SE/USER/HUTE/SCHEM/HS_DRAW/HSPEED2 8.DRAW

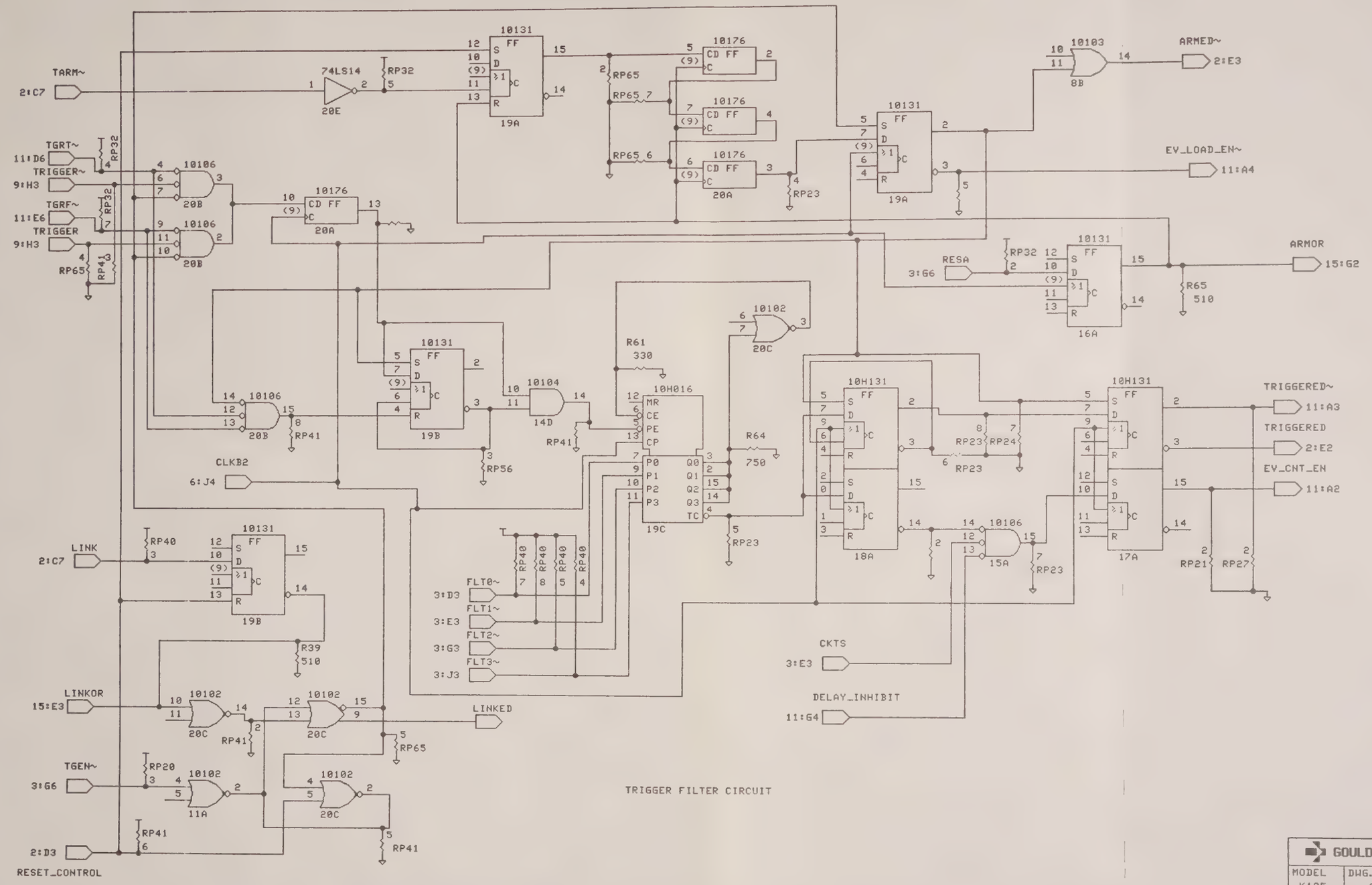


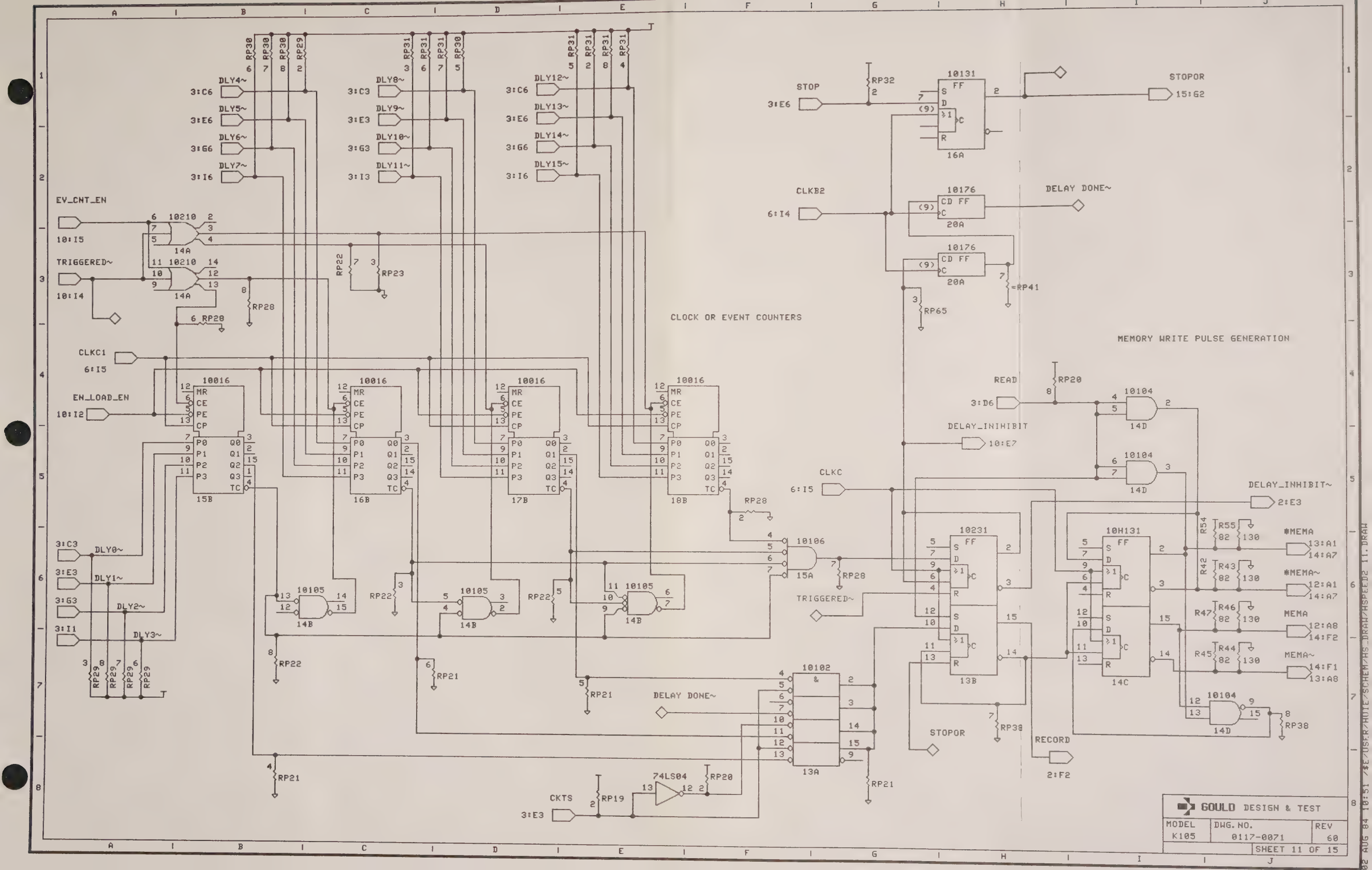


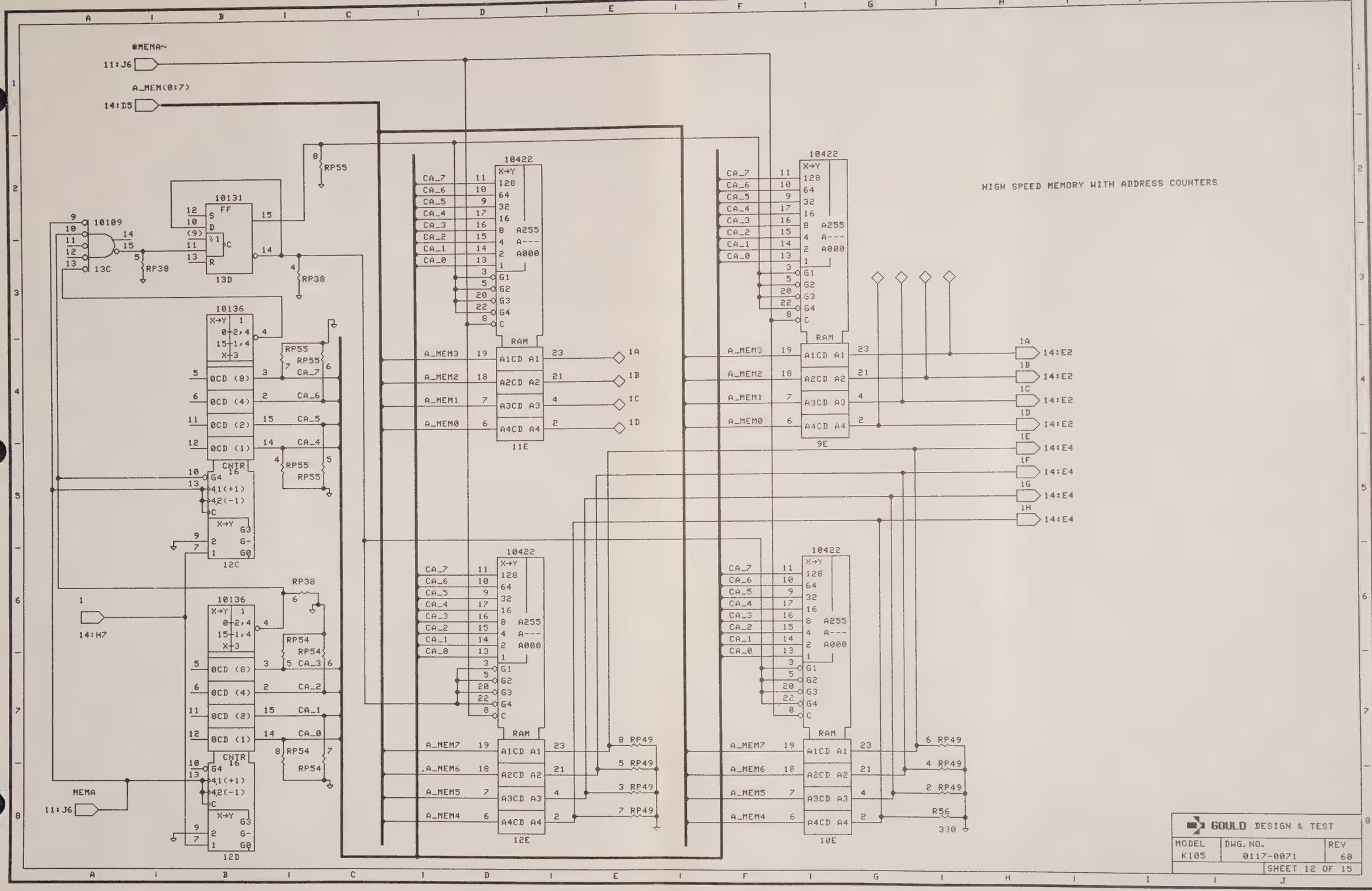


GOULD DESIGN & TEST		
MODEL K105	DWG. NO. 0117-0071	REV 60
	SHEET 9 OF 15	

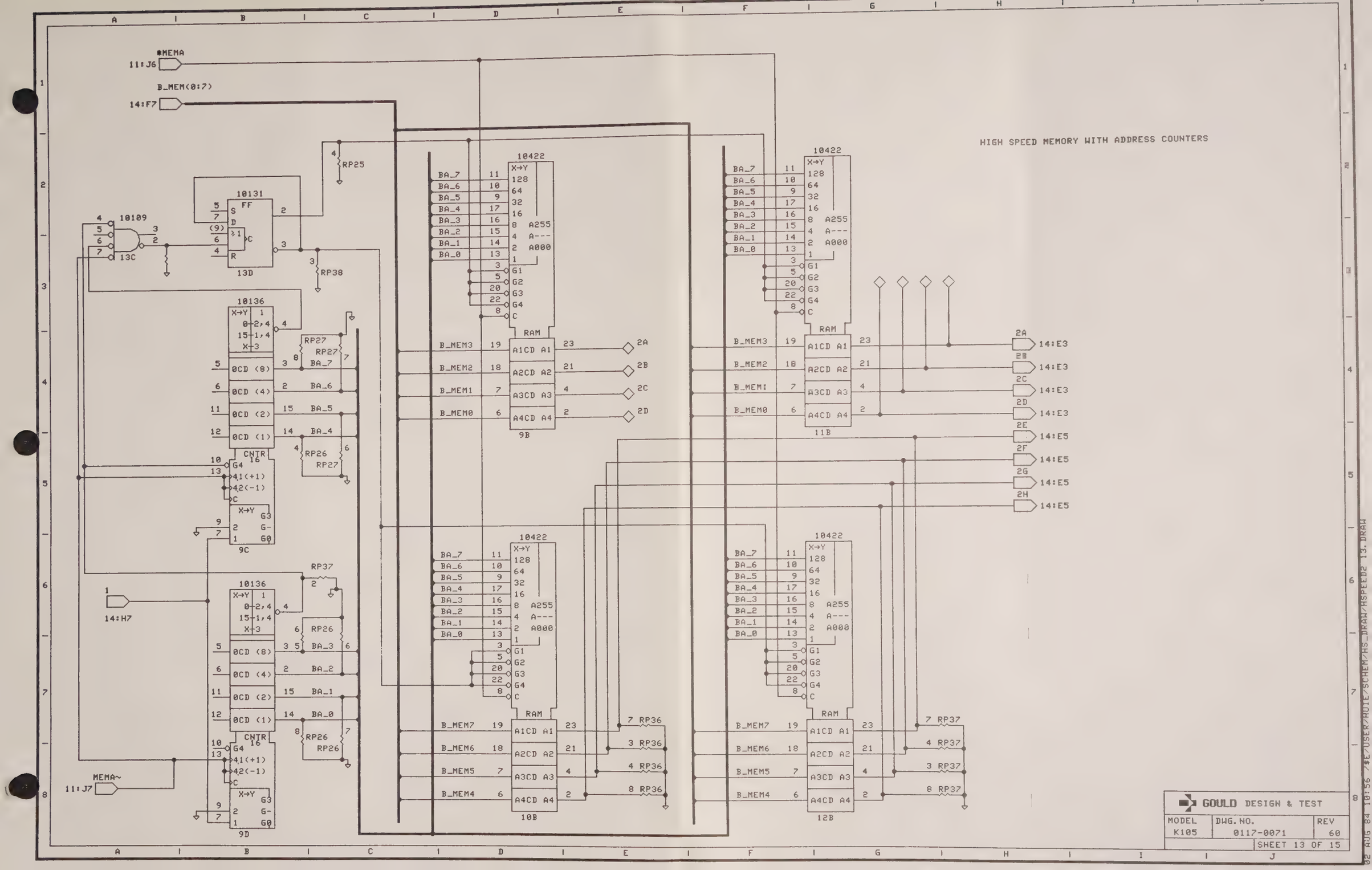
02 AUG 84 10:47 /*E/USER/HUTE/SCHEM/HS_DRAW/HSPEED2 9.DRAW

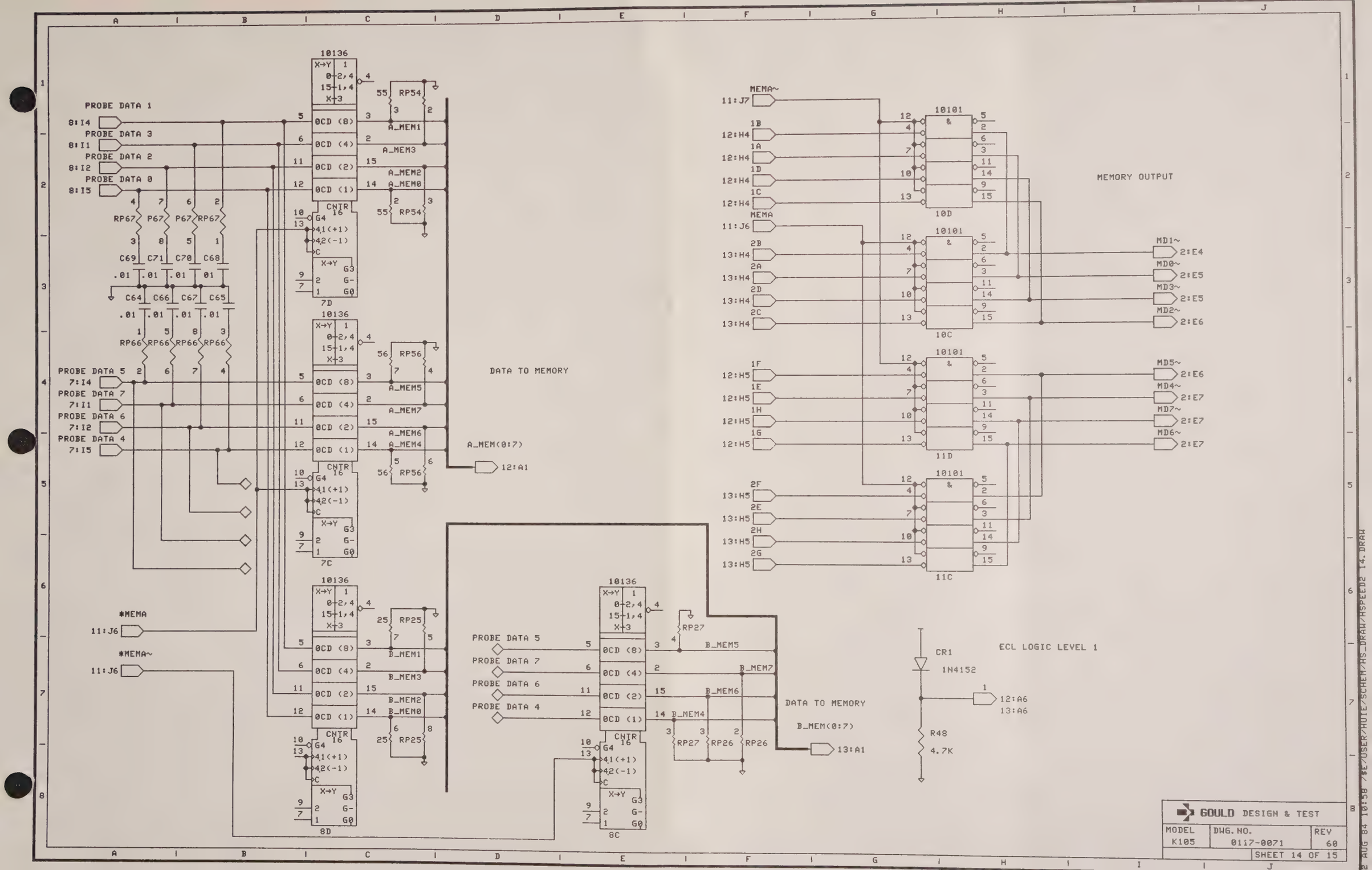

TARM~
2:C7
74LS14
20E
RP32
10131
FF
19A
RP65
10176
CD FF
20A
RP23
10103
8B
ARMED~
2:E3
EV_LOAD_EN~
11:A4
TGRT~
11:D6
TRIGGER~
9:H3
TGRF~
11:E6
TRIGGER
9:H3
10106
20B
RP65
RP41
RESA
3:G6
ARMOR
15:G2
R65
510
16A
R61
330
10102
20C
10H016
19C
R64
750
RP56
14D
10104
CLKB2
6:J4
10H131
18A
17A
TRIGGERED~
11:A3
TRIGGERED
2:E2
EV_CNT_EN
11:A2
RP21
RP27
15A
LINK
2:C7
RP40
19B
R39
510
FLT0~
3:D3
FLT1~
3:E3
FLT2~
3:G3
FLT3~
3:J3
CKTS
3:E3
DELAY_INHIBIT
11:G4
LINKOR
15:E3
LINKED
RP20
11A
TGEN~
3:G6
2:D3
RESET_CONTROL
TRIGGER FILTER CIRCUIT
GOULD DESIGN & TEST
MODEL K105
DWG. NO. 0117-0071
REV 60
SHEET 10 OF 15
02 AUG 84 10:49 /SE/USER/HUIE/SCHEM/HS_DRAW/HSPLED2_10.DRAW

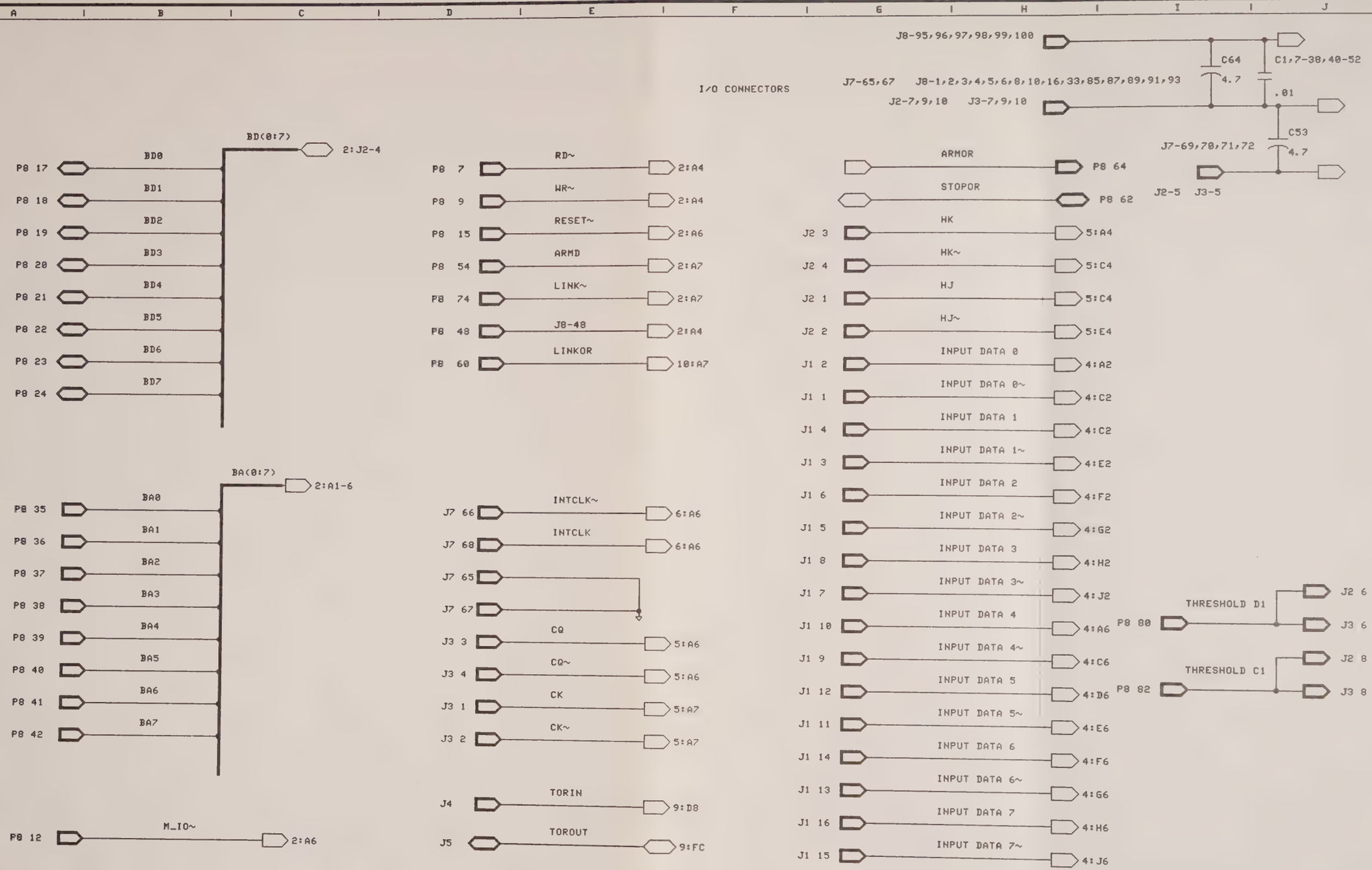

CLOCK OR EVENT COUNTERS
MEMORY WRITE PULSE GENERATION
EV_CNT_EN
10:I5
TRIGGERED~
10:I4
CLKC1
6:I5
EN_LOAD_EN
10:I2
DLY0~
DLY1~
DLY2~
DLY3~
DLY4~
DLY5~
DLY6~
DLY7~
DLY8~
DLY9~
DLY10~
DLY11~
DLY12~
DLY13~
DLY14~
DLY15~
STOP
3:E6
STOPOR
15:G2
CLKB2
6:I4
DELAY DONE~
READ
3:D6
DELAY_INIHIBIT
10:E7
CLKC
6:I5
DELAY_INHIBIT~
2:E3
TRIGGERED~
DELAY DONE~
STOPOR
RECORD
2:F2
CKTS
3:E3
*MEMA
13:A1
14:A7
*MEMA~
12:A1
14:A7
MEMA
12:A8
14:F2
MEMA~
14:F1
13:A8
10131
10176
10210
10016
10105
10106
10102
10231
10H131
10104
74LS04
GOULD DESIGN & TEST
MODEL K105
DWG. NO. 0117-0071
REV 60
SHEET 11 OF 15



GOULD DESIGN & TEST		
MODEL K105	DWG. NO. 0117-0071	REV 60
		SHEET 12 OF 15

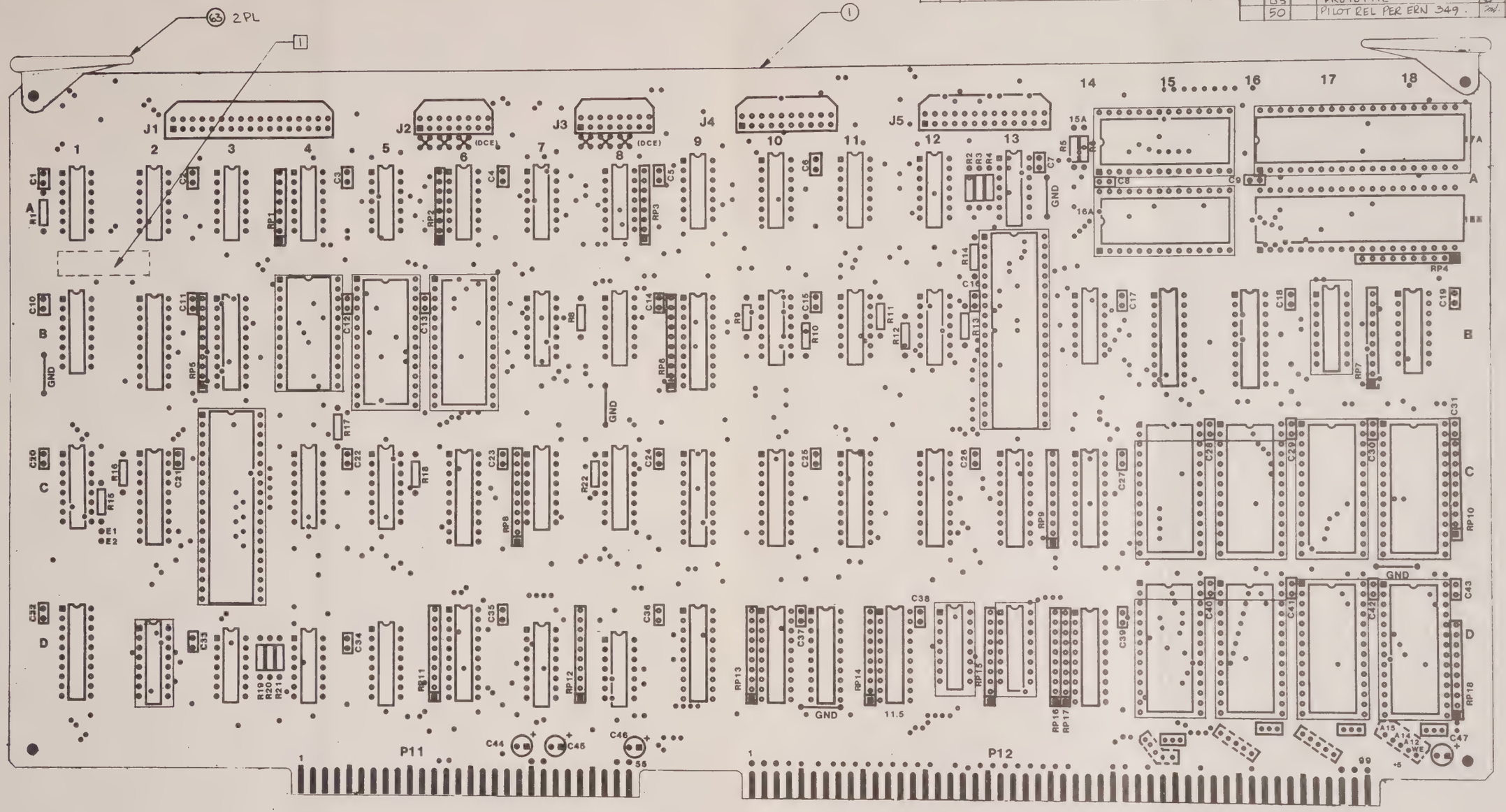

HIGH SPEED MEMORY WITH ADDRESS COUNTERS
*MEMA
11:J6
B_MEM(0:7)
14:F7
MEMA~
11:J7
14:H7
10109
13C
10131
FF
13D
RP25
RP38
10136
CNTR
9C
RP27
RP26
RP37
9D
10422
RAM
9B
10B
11B
12B
BA_7
BA_6
BA_5
BA_4
BA_3
BA_2
BA_1
BA_0
B_MEM3
B_MEM2
B_MEM1
B_MEM0
B_MEM7
B_MEM6
B_MEM5
B_MEM4
2A
2B
2C
2D
2E
2F
2G
2H
14:E3
14:E5
RP36
RP37
GOULD DESIGN & TEST
MODEL K105
DWG. NO. 0117-0071
REV 60
SHEET 13 OF 15


PROBE DATA 1
8:I4
PROBE DATA 3
8:I1
PROBE DATA 2
8:I2
PROBE DATA 0
8:I5
PROBE DATA 5
7:I4
PROBE DATA 7
7:I1
PROBE DATA 6
7:I2
PROBE DATA 4
7:I5
10136
7D
7C
8D
8C
RP54
RP56
RP25
RP67
RP66
C64
C66
C67
C65
C69
C71
C70
C68
A_MEM1
A_MEM3
A_MEM2
A_MEM0
A_MEM5
A_MEM7
A_MEM6
A_MEM4
A_MEM(0:7)
12:A1
DATA TO MEMORY
B_MEM1
B_MEM3
B_MEM2
B_MEM0
B_MEM5
B_MEM7
B_MEM6
B_MEM4
B_MEM(0:7)
13:A1
RP27
RP26
*MEMA
11:J6
*MEMA~
11:J6
MEMA~
11:J7
MEMA
11:J6
10101
10D
10C
11D
11C
MEMORY OUTPUT
MD1~
2:E4
MD0~
2:E5
MD3~
2:E5
MD2~
2:E6
MD5~
2:E6
MD4~
2:E7
MD7~
2:E7
MD6~
2:E7
CR1
1N4152
R48
4.7K
ECL LOGIC LEVEL 1
12:A6
13:A6
GOULD DESIGN & TEST
MODEL K105
DWG. NO. 0117-0071
REV 60
SHEET 14 OF 15


I/O CONNECTORS
BD(0:7)
P8 17 BD0
P8 18 BD1
P8 19 BD2
P8 20 BD3
P8 21 BD4
P8 22 BD5
P8 23 BD6
P8 24 BD7
2:J2-4
BA(0:7)
P8 35 BA0
P8 36 BA1
P8 37 BA2
P8 38 BA3
P8 39 BA4
P8 40 BA5
P8 41 BA6
P8 42 BA7
2:A1-6
P8 12 M_IO~
2:A6
P8 7 RD~
P8 9 WR~
P8 15 RESET~
P8 54 ARMD
P8 74 LINK~
P8 48 J8-48
P8 60 LINKOR
2:A4
2:A4
2:A6
2:A7
2:A7
2:A4
10:A7
J7 66 INTCLK~
J7 68 INTCLK
J7 65
J7 67
J3 3 CQ
J3 4 CQ~
J3 1 CK
J3 2 CK~
6:A6
6:A6
5:A6
5:A6
5:A7
5:A7
J4 TORIN
J5 TOROUT
9:D8
9:FC
J8-95,96,97,98,99,100
J7-65,67 J8-1,2,3,4,5,6,8,10,16,33,85,87,89,91,93
J2-7,9,10 J3-7,9,10
C64 4.7
C1,7-38,40-52
.01
C53 4.7
J7-69,70,71,72
J2-5 J3-5
P8 64 ARMOR
P8 62 STOPOR
J2 3 HK
J2 4 HK~
J2 1 HJ
J2 2 HJ~
J1 2 INPUT DATA 0
J1 1 INPUT DATA 0~
J1 4 INPUT DATA 1
J1 3 INPUT DATA 1~
J1 6 INPUT DATA 2
J1 5 INPUT DATA 2~
J1 8 INPUT DATA 3
J1 7 INPUT DATA 3~
J1 10 INPUT DATA 4
J1 9 INPUT DATA 4~
J1 12 INPUT DATA 5
J1 11 INPUT DATA 5~
J1 14 INPUT DATA 6
J1 13 INPUT DATA 6~
J1 16 INPUT DATA 7
J1 15 INPUT DATA 7~
5:A4
5:C4
5:C4
5:E4
4:A2
4:C2
4:C2
4:E2
4:F2
4:G2
4:H2
4:J2
4:A6
4:C6
4:D6
4:E6
4:F6
4:G6
4:H6
4:J6
P8 80 THRESHOLD D1
J2 6
J3 6
P8 82 THRESHOLD C1
J2 8
J3 8
GOULD DESIGN & TEST
MODEL K105
DWG. NO. 6117-0071
REV 60
SHEET 15 OF 15
AUG 84 11:01 /#:/USER/ROUTE/SCHEM/HS_DRAW/HSPEED2 15.DRAW

ZONE	REV	ECO	DESCRIPTION	DWN	CHKD	DATE
	STRT	4264	REVISED PER ECO N°	JWC	[illegible]	1-23-84
	A	4409	PROD REL PER ECO	D.C.	[illegible]	03-15-84

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	02		PROTOTYPE	M.W	—	—
	03		PROTOTYPE	[illegible]	—	—
	50		PILOT REL PER ERN 349.	[illegible]	—	—



COMPONENT SIDE

NOTES: UNLESS OTHERWISE SPECIFIED

1. STAMP ASSEMBLY DASH NO., REVISION LEVEL AND SERIAL NO. APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK.
2. ASSEMBLY REFLECTS SCHEMATIC DRAWING 0117-0076 AND FABRICATION DRAWING 0117-0077.

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 | ANGLES ± 1° | XX ± .020 | XXX ± .010

HOLE SIZE: 0 .599 - .003 | 600 .999 - .004 | 1.000 1.499 - .005

DASH NO	NUMBER	QTY
10	0117-0003	1
	NEXT ASSEMBLY	

		DATE
DRAWN	M. W	12/7/82
CHECKED	[signature]	1/3/83
PROJ ENG	[signature]	1/3/83
MANUFACTURING	[signature]	1/17/83
QUALITY ASSUR	[signature]	2/2/83
ENG SERV		DATE

GOULD Instruments Division Santa Clara Operations

TITLE: ASSEMBLY I/O

SCALE	SIZE	PART NUMBER	REV
2/1	D	0117-0075	A

MODEL: K105 SHEET 1 OF 1

ITEM	QUANTITY PER ASSEMBLY -80	-70	-60	-50	-40	-30	-20	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1								—	1	0117-0077	PCB, I/O		
2								—	REF	0117-0076	SCHEMATIC, I/O		
3								—	2	1800-0105	74LS00	12A, 12B	
4								—	3	-0298	74LS373	16B, 9C, 11C	
5								—	1	0107	74LS04	13A	
6								—	1	0097	7406	1A	
7								—	2	0085	7407	2A, 9A	
8								—	2	0243	74 S08	11A, 8D	
9								—	3	0216	74LS32	8B, 11B, 14B	
10								—	1	0347	74LS33	8A	
11								—	1	0311	7438	3A	
12								—	4	0115	74LS74	7B, 10B, 3D, 4D	
13								—	1	0117	74LS86	10A	
14								—	1	0237	74LS139	1B	
15								—	1	0312	74 S138	7C	
16								—	1	0181	74LS151	1C	
17								—	2	0125	74LS161	4C, 5C	
18								—	3	0267	74LS240	2B, 3B, 9B	
19								—	2	0240	74LS244	6D, 9D	
20								—	6	0268	74LS245	13C, 14C, 10D, 11D, 11-5D, 14D	
21								—	2	0277	74LS257	5D, 7D	
22								—	2	0231	74LS273	2C, 1D	
23								—	4	0293	74LS374	15B, 6C, 10C, 12C	
24								—	2	0278	74LS155	8C, 18B	
25								2	—	0343	8251-A	5B, 6B	
26								1	—	0344	8253-5	4B	
27								1	—	1800 — 0342	8272	3C	

REV	DESCRIPTION	DATE	DWN	CKD
02	PROTO	12/17/82	MW	1/3/83
03	PRODUCTION TYPE	1/19/83		
50	PILOT REL PER ECN 349	4-12-83	MW	
57	REV'D PER ECO#264	1/23/84	DSW	DSW MW
A	PROD REL ECO 4409	2/22/84	D.C.	DSW

DASH NO.	NEXT ASSEMBLY NUMBER	QTY
05	0117-0075-05	1
10	0117-0003	1

		DATE
DWN	J.W. CARROLL	10-29-82
CHK		1/3/83
ENGR		5/3/83
MFG.		5/3/83
Q.A.		5/3/83

LIST OF MATERIAL
ASSEMBLY
I/O

GOULD biomation

B | 0117-0075 | REV A

MODEL K105 | SHEET 1 OF 3

KLINGLER K-VEL H-10

ITEM	QUANTITY PER ASSEMBLY -80	-70	-60	-50	-40	-30	-20	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
28								1	—	1800-0358	8257	13B	
29								1	—	-0527	8291	17A	
30								—	—	-0528	8292	18A (NOT USED ON -10)	
31								2	—	-0529	8293	15A 16A	
32													
33													
34								—	2	1700-0101	1488	5A, 7A	
35								—	2	1700-0128	1489A	4A, 6A	
36													
37								1	—	0117-0217-01	SPEC PROM MAIN I/O DECODE	13D	
38								1	—	0117-0218-01	SPEC PROM K105 LATCH I/O DECODE	12D	
39								1	—	0117-0219-01	SPEC PROM K105 I/O BD MEM DECODE	17B	
40								1	—	0117-022D-01	SPEC PROM K105 I/O DOS PLL	2D	
41								4	—	1820-0080	2K X 8 ST RAM CMOS	15C, 16C, 15D, 16D (REF 6116)	
42													
43													
44								—	18	3100-2001	RESISTOR, 2K, 1/8W, 1%, MF	R1, R4-R6, R8-R10, R12-R22	
45								—	2	-4750	RESISTOR, 475Ω, 1/8W, 1%, MF	R2, R3	
46								—	1	3100-6190	RESISTOR, 619Ω, 1/8W, 1%, MF	R11	
47													
48													
49								—	2	3700-0041	RESISTOR PAK, 4.7K, 2W, 2%, 8P	RP1, 2	
50								—	14	0049	R PAK, 3K/6.2K, 1/8W, 5%, 10P	RP4, 6-18	
51								—	1	0065	R PAK, 220/330, 1/8W, 5%, 10P	RP5	
52								—	1	3700-0069	R PAK, 2K, .2W, 2%, 8/7R	RP3	
53													
54								—	43	4010-0103	CAPACITOR, .01 μf, 50V, 10%	C1-43	
55													
56								—	2	4400-0043	CAPACITOR, 47μf, 6V	C46, 47	
57								—	2	4400-0045	CAPACITOR, 33μf, 25V	C44, 45	

NOTES

LIST OF MATERIAL
ASSEMBLY
I/O

GOULD biomation

B | 0117-0075 | REV A

MODEL K105 | SHEET 2 OF 3

KLINGLER K-VEL H-10

ITEM	QUANTITY PER ASSEMBLY -60	-70	-50	-60	-40	-30	-20	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
58								—	2	6000-0374	CONNECTOR, 16 PIN, HDR, RT. ANGL	J 2,3	
59								—	—	-0372	" 20 POS, HDR, RT. ANGL	J4 (NOT USED ON -05)	
60								—	1	-0388-20	" 26 PIN, RT. ANGL, HDR	J5	
61								—	1	6000-0373	CONNECTOR, 34 POS, HDR, RT. ANG	J1	
62													
63								—	2	7000-0120	CARD EJECTOR, NYLON 6/6		
64													
65								—	4	6100-0023	SOCKET, 16 PIN, LO PRO	2D, 12D, 13D, 17B	
66								—	5	6100-0122	" 24 PIN, "	4B, 15C, 16C, 15D, 16D	
67								—	8	6100-0151	" 28 PIN, LO PRO	5B, 6B, 17C, 18C, 17D, 18D, 15A, 16A	
68								—	3	6100-0123	SOCKET, 40 PIN,	3C, 13B, 17A	
69													
70								—	4	9000-0054	BUS WIRE, FORMED	GND	
71													
72								1	—	0117-0175-00	ASSY, 4 PROM SET, I/O		
73								REF	—	0117-0175-01	ASSY PROM 1 OF 4	17C	
74								REF	—	0117-0175-02	ASSY PROM 2 OF 4	17D	
75								REF	—	0117 0175-03	ASSY PROM 3 OF 4	18C	
76								REF	—	0117-0175-04	ASSY PROM 4 OF 4	18D	
77													
78								1	—	0117-0075-05	I/O PCBA		
79													
80													
81													
82													
83													
84													
85													
86													
87													

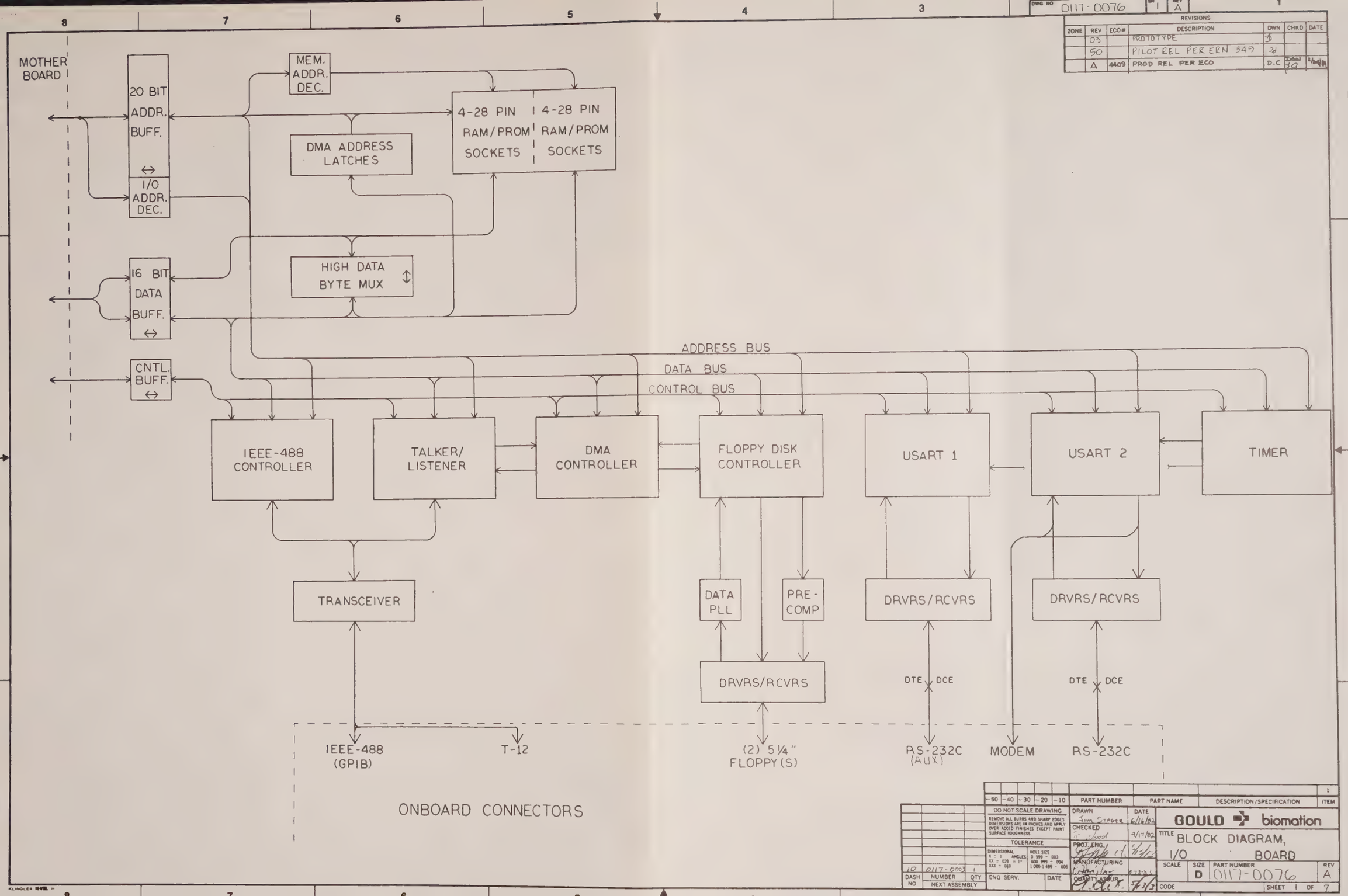
NOTES

LIST OF MATERIAL
ASSEMBLY
I/O

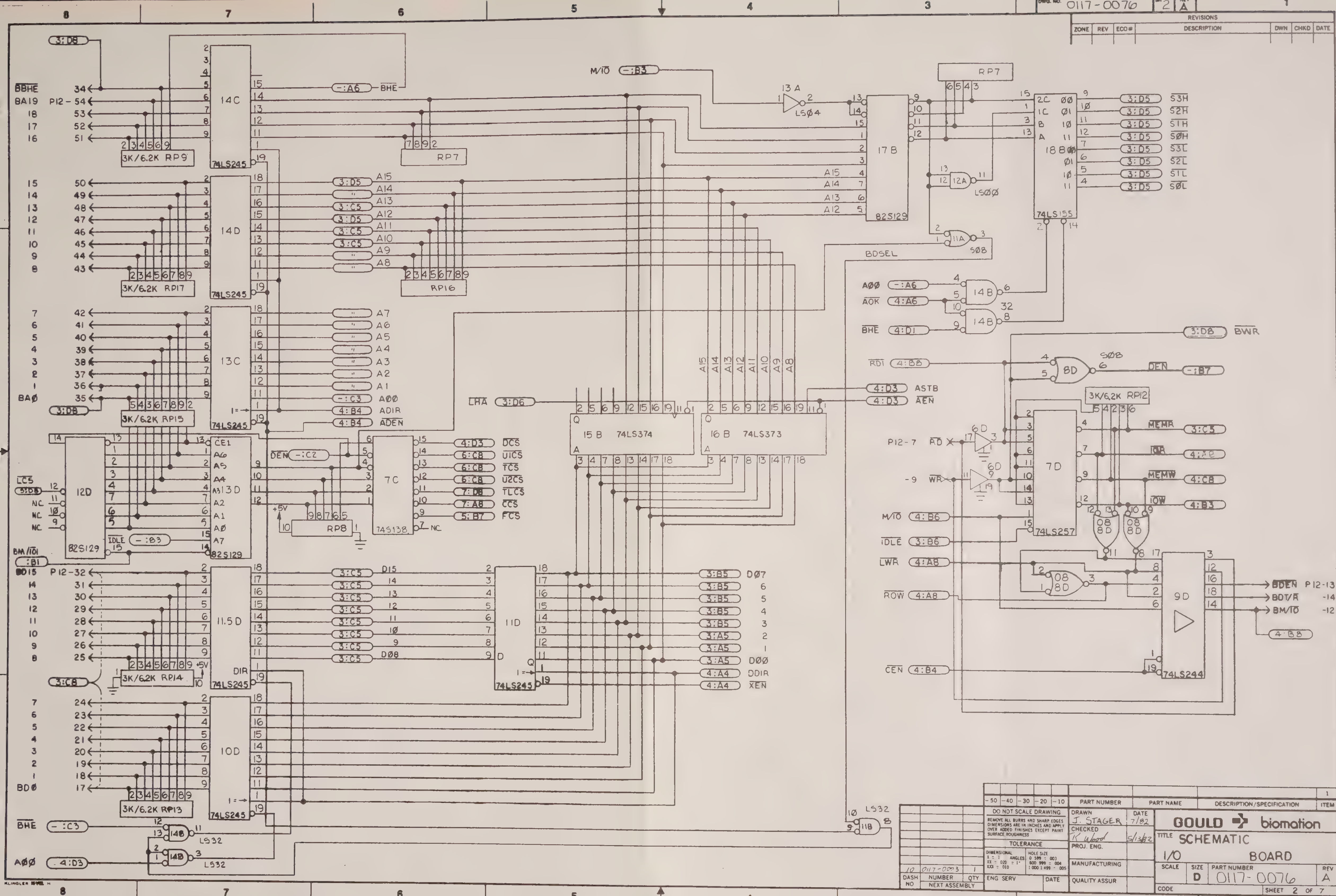
GOULD biomation

B	0117-0075	REV A
MODEL K105	SHEET 3 OF 3	

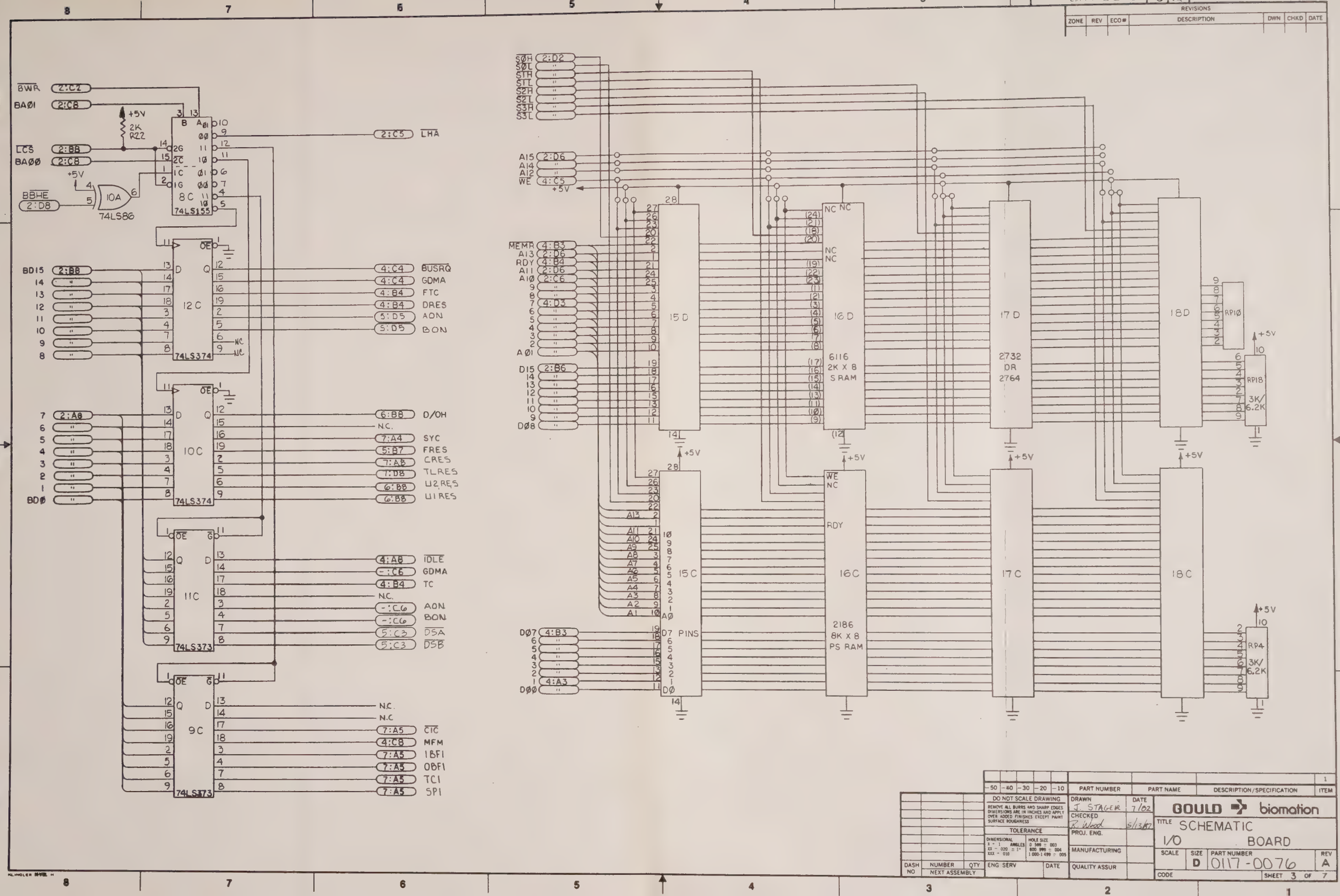
KLINGLER K-VEL H-10



DWG NO 0117-0076
SH 1
REV A
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
03 | PROTOTYPE
50 | PILOT REL PER ERN 349
A | 4409 | PROD REL PER ECO | D.C
MOTHER BOARD
20 BIT ADDR. BUFF.
I/O ADDR. DEC.
MEM. ADDR. DEC.
DMA ADDRESS LATCHES
4-28 PIN RAM/PROM SOCKETS
4-28 PIN RAM/PROM SOCKETS
HIGH DATA BYTE MUX
16 BIT DATA BUFF.
CNTL. BUFF.
ADDRESS BUS
DATA BUS
CONTROL BUS
IEEE-488 CONTROLLER
TALKER/ LISTENER
DMA CONTROLLER
FLOPPY DISK CONTROLLER
USART 1
USART 2
TIMER
TRANSCEIVER
DATA PLL
PRE-COMP
DRVRS/RCVRS
DRVRS/RCVRS
DRVRS/RCVRS
DTE DCE
DTE DCE
IEEE-488 (GPIB)
T-12
(2) 5¼" FLOPPY(S)
RS-232C (AUX)
MODEM
RS-232C
ONBOARD CONNECTORS
-50 -40 -30 -20 -10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL X = 1 ANGLES XX = .020 ± 1° XXX = .010
HOLE SIZE 0.599 - .003 .600 .999 - .004 1.000-1.499 - .005
DRAWN Jim Stager 6/16/82
CHECKED 9/17/82
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR.
GOULD biomation
TITLE BLOCK DIAGRAM, I/O BOARD
SCALE
SIZE D
PART NUMBER 0117-0076
REV A
CODE
SHEET 1 OF 7
10 0117-0003 1
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV.
DATE



0117-0076
2
A
REVISIONS
ZONE
REV
ECO #
DESCRIPTION
DWN
CHKD
DATE
14C
74LS245
14D
74LS245
13C
74LS245
12D
82S129
13D
82S129
11.5D
74LS245
10D
74LS245
11D
74LS245
7C
74S138
15 B 74LS374
16 B 74LS373
17 B
82S129
18 B
74LS155
7D
74LS257
9D
74LS244
3K/6.2K RP9
3K/6.2K RP17
3K/6.2K RP15
3K/6.2K RP14
3K/6.2K RP13
3K/6.2K RP12
RP7
RP16
RP8
M/IO
BDSEL
BHE
LHA
ASTB
AEN
DEN
BWR
MEMR
IOR
MEMW
IOW
BDEN P12-13
BOT/R -14
BM/IO -12
DCS
U1CS
TCS
U2CS
TLCS
CCS
FCS
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
J. STAGER
DATE
7/82
CHECKED
5/13/82
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
GOULD biomation
TITLE SCHEMATIC
I/O BOARD
SCALE
SIZE
D
PART NUMBER
0117-0076
REV
A
CODE
SHEET 2 OF 7
10
0117-0003
DASH NO
NUMBER
QTY
NEXT ASSEMBLY



REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, ANGLES ±2°, .XX ± .020, .XXX ± .010
HOLE SIZE: 0 to .599 ± .003; .600 to .999 ± .004; 1.000 to 1.499 ± .005

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG SERV | DATE

MANUFACTURING

QUALITY ASSUR

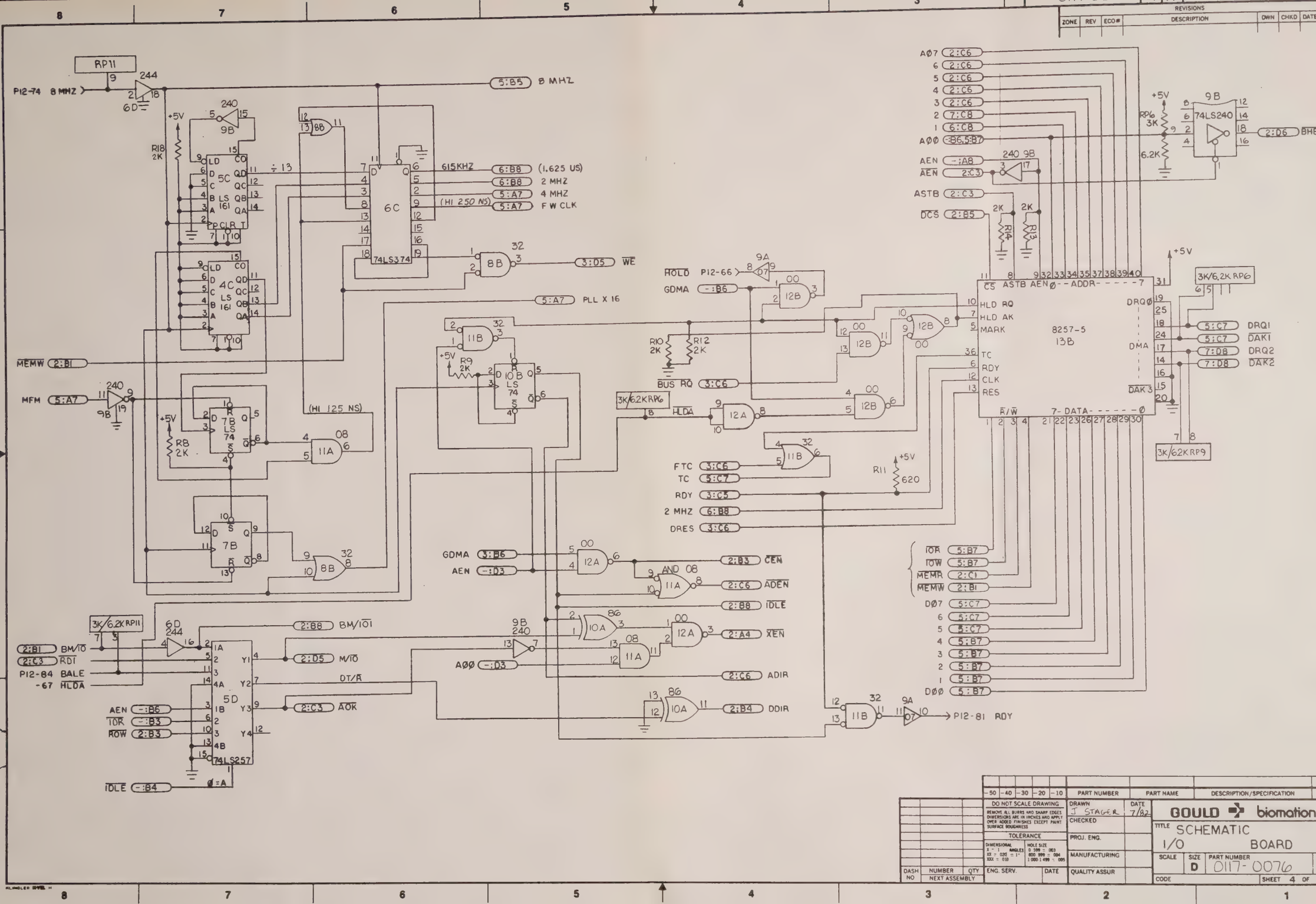
DRAWN	DATE
J. STAGER	7/82
CHECKED	
R. Wood	8/13/82
PROJ. ENG.	

GOULD biomation

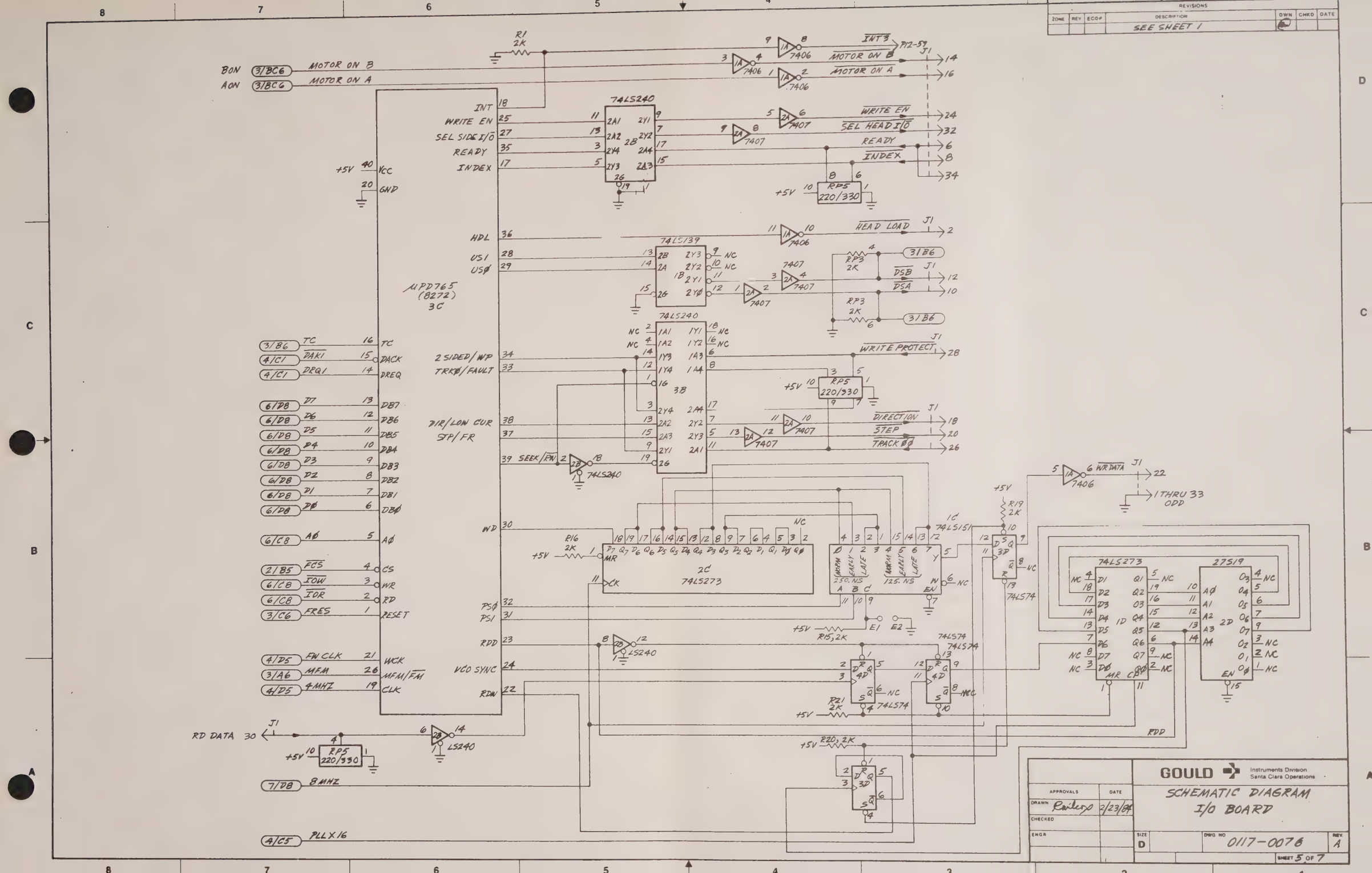
TITLE: SCHEMATIC I/O BOARD

SCALE	SIZE	PART NUMBER	REV
	D	0117-0076	A

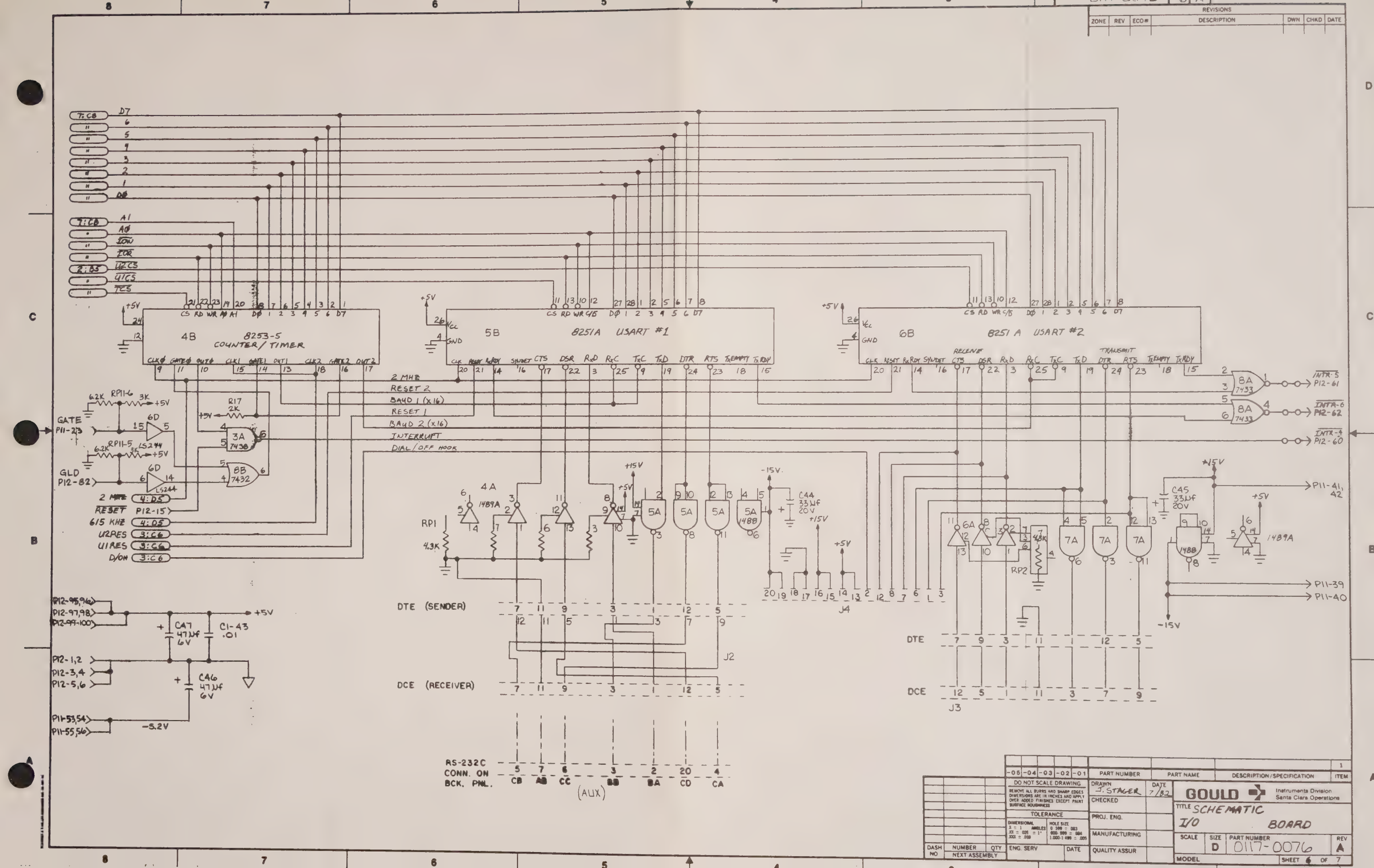
CODE | SHEET 3 OF 7

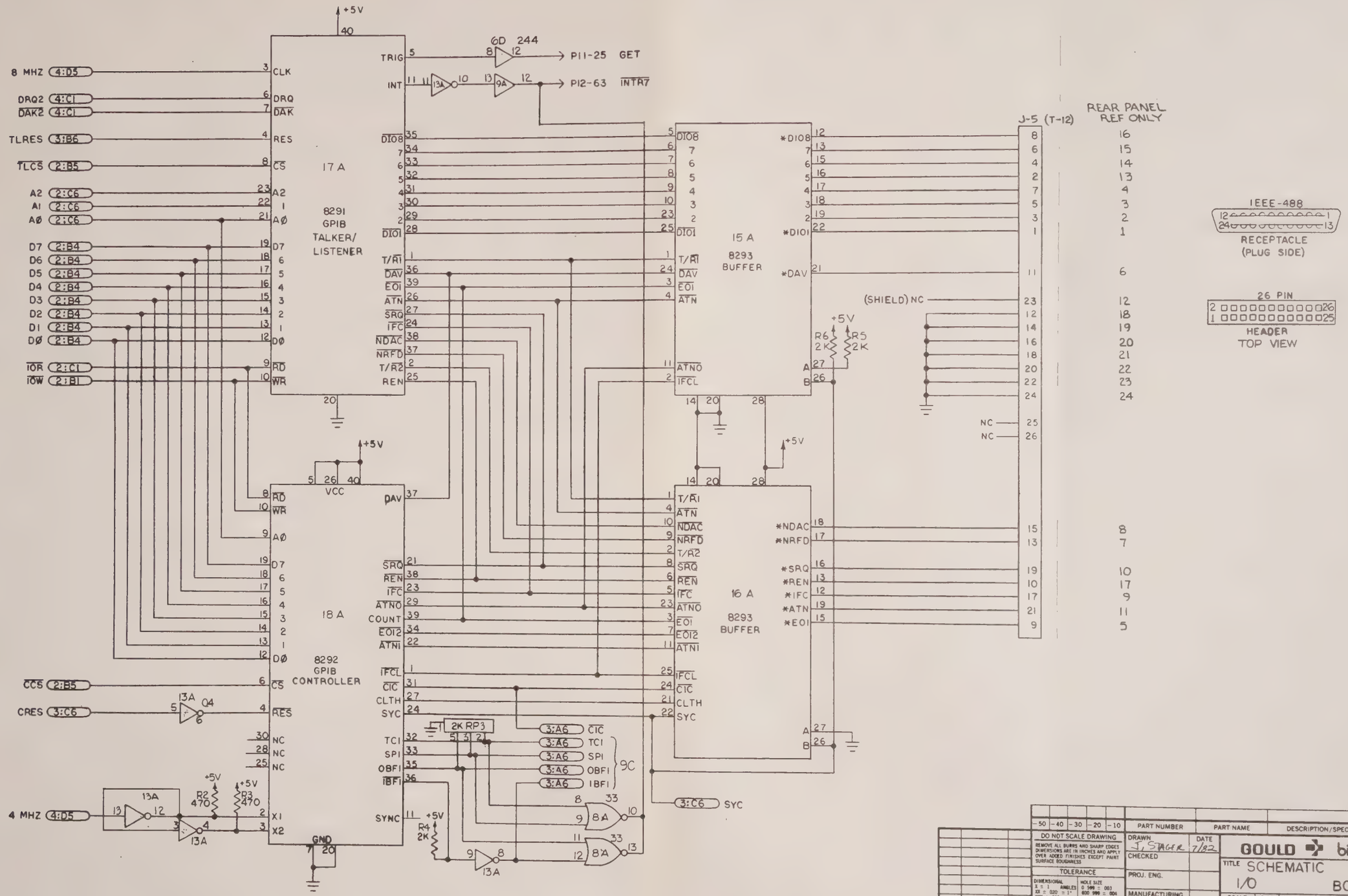


RP11
P12-74 8 MHZ
244
6D
5:B5 8 MHZ
240
9B
R18 2K
+5V
5C
LS 161
4C
LS 161
÷ 13
615KHZ
6:B8 (1.625 US)
6:B8 2 MHZ
5:A7 4 MHZ
(HI 250 NS) 5:A7 F W CLK
6C
74LS374
8B
32
3:D5 WE
5:A7 PLL X 16
MEMW 2:B1
MFM 5:A7
240
9B
R8 2K
7B
LS 74
(HI 125 NS)
11A
08
7B
8B
32
11B
32
R9 2K
10B
LS 74
HOLD P12-66
GDMA -:B6
9A
12B
00
R10 2K
R12 2K
BUS RQ 3:C6
3K/6.2KRP6
HLDA
12A
11B
32
FTC 3:C6
TC 5:C7
RDY 3:C5
2 MHZ 6:B8
DRES 3:C6
R11 620
GDMA 3:B6
AEN -:D3
12A
00
AND 08
11A
2:B3 CEN
2:C6 ADEN
2:B8 IDLE
10A
86
12A
00
11A
08
2:A4 XEN
2:C6 ADIR
2:B4 DDIR
AØØ -:D3
9B
240
2:B8 BM/IOI
2:D5 M/IO
DT/R
2:C3 AOK
3K/6.2KRP11
6D
244
2:B1 BM/IO
2:C3 RDI
P12-84 BALE
-67 HLDA
5D
74LS257
AEN -:B6
IOR -:B3
ROW 2:B3
IDLE -:B4
Ø=A
11B
32
9A
P12-81 RDY
AØ7 2:C6
6 2:C6
5 2:C6
4 2:C6
3 2:C6
2 7:C8
1 6:C8
AØØ -:B6,5:B7
AEN -:A8
AEN 2:C3
240 9B
ASTB 2:C3
DCS 2:B5
2K
R14
2K
R13
+5V
RP6 3K
6.2K
9B
74LS240
2:D6 BHE
8257-5
13B
CS ASTB AEN Ø - - ADDR - - - - 7
HLD RQ
HLD AK
MARK
TC
RDY
CLK
RES
DRQØ
DMA
DAK3
R/W
7- DATA - - - - - Ø
3K/6.2K RP6
5:C7 DRQ1
5:C7 DAK1
7:D8 DRQ2
7:D8 DAK2
3K/6.2K RP9
IOR 5:B7
IOW 5:B7
MEMR 2:C1
MEMW 2:B1
DØ7 5:C7
6 5:C7
5 5:C7
4 5:B7
3 5:B7
2 5:B7
1 5:B7
DØØ 5:B7
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL X = 1 ANGLES XX = .020 ± 1° XXX = .010
HOLE SIZE 0.599 ± .003 .800 .999 ± .004 1.000-1.499 ± .005
DRAWN J STAGER DATE 7/82
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV. DATE
DASH NO NUMBER QTY NEXT ASSEMBLY
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
GOULD biomation
TITLE SCHEMATIC I/O BOARD
SCALE SIZE D PART NUMBER 0117-0076 REV A
CODE SHEET 4 OF 7



REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHEET 1
BON 3/BC6 MOTOR ON B
AON 3/BC6 MOTOR ON A
R1 2K
INT3 P12-59
MOTOR ON B
MOTOR ON A
74LS240
WRITE EN
SEL HEAD I/O
READY
INDEX
RP5 220/330
HEAD LOAD
74LS139
RP3 2K
DSB
DSA
3/B6
74LS240
WRITE PROTECT
DIRECTION
STEP
TRACK ØØ
μPD765 (8272) 3C
INT
WRITE EN
SEL SIDE I/O
READY
INDEX
HDL
US1
USØ
2 SIDED/WP
TRKØ/FAULT
DIR/LOW CUR
STP/FR
SEEK/RW
WD
PSØ
PS1
RDD
VCO SYNC
RDW
TC
DACK
DREQ
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
AØ
CS
WR
RD
RESET
WCK
MFM/FM
CLK
FCS
IOW
IOR
FRES
FW CLK
MFM
4MHZ
RD DATA 30
8MHZ
PLL X16
74LS273
74LS151
74LS74
27S19
WR DATA
1 THRU 33 ODD
R16 2K
R19 2K
R15, 2K
R21 2K
R20, 2K
LS240
GOULD Instruments Division Santa Clara Operations
SCHEMATIC DIAGRAM I/O BOARD
APPROVALS DATE
DRAWN 2/23/84
CHECKED
ENGR
SIZE D
DWG NO 0117-0076
REV A
SHEET 5 OF 7


REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
4B 8253-5 COUNTER/TIMER
5B 8251A USART #1
6B 8251A USART #2
RECEIVE
TRANSMIT
2 MHz
RESET 2
BAUD 1 (x16)
RESET 1
BAUD 2 (x16)
INTERRUPT
DIAL/OFF HOOK
GATE P11-23
GLD P12-82
2 MHz
RESET P12-15
615 KHz
U2RES
U1RES
D/ON
INTR-5 P12-61
INTR-6 P12-62
INTR-7 P12-60
P11-41, 42
P11-39
P11-40
DTE (SENDER)
DCE (RECEIVER)
J2
J3
J4
DTE
DCE
RS-232C CONN. ON BCK. PNL.
(AUX)
P12-95,96
P12-97,98
P12-99-100
P12-1,2
P12-3,4
P12-5,6
P11-53,54
P11-55,56
-5.2V
PART NUMBER | PART NAME | DESCRIPTION/SPECIFICATION | ITEM
DRAWN J. STAGER DATE 7/82
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
GOULD Instruments Division Santa Clara Operations
TITLE SCHEMATIC I/O BOARD
SCALE D PART NUMBER 0117-0076 REV A
MODEL SHEET 6 OF 7
DO NOT SCALE DRAWING
TOLERANCE
DASH NO | NUMBER | QTY
NEXT ASSEMBLY
ENG. SERV | DATE



ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DWG. NO.	REV
0117-0076	A

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER
1			

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY
OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1; XX ± .020 = 1°; XXX ± .010

HOLE SIZE: 0 .999 = .003; .000 .999 = .004; 1.000 1.499 = .005

DRAWN	J. STAGER 7/82
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR	
ENG SERV	DATE

GOULD biomation

TITLE SCHEMATIC 1/0 BOARD

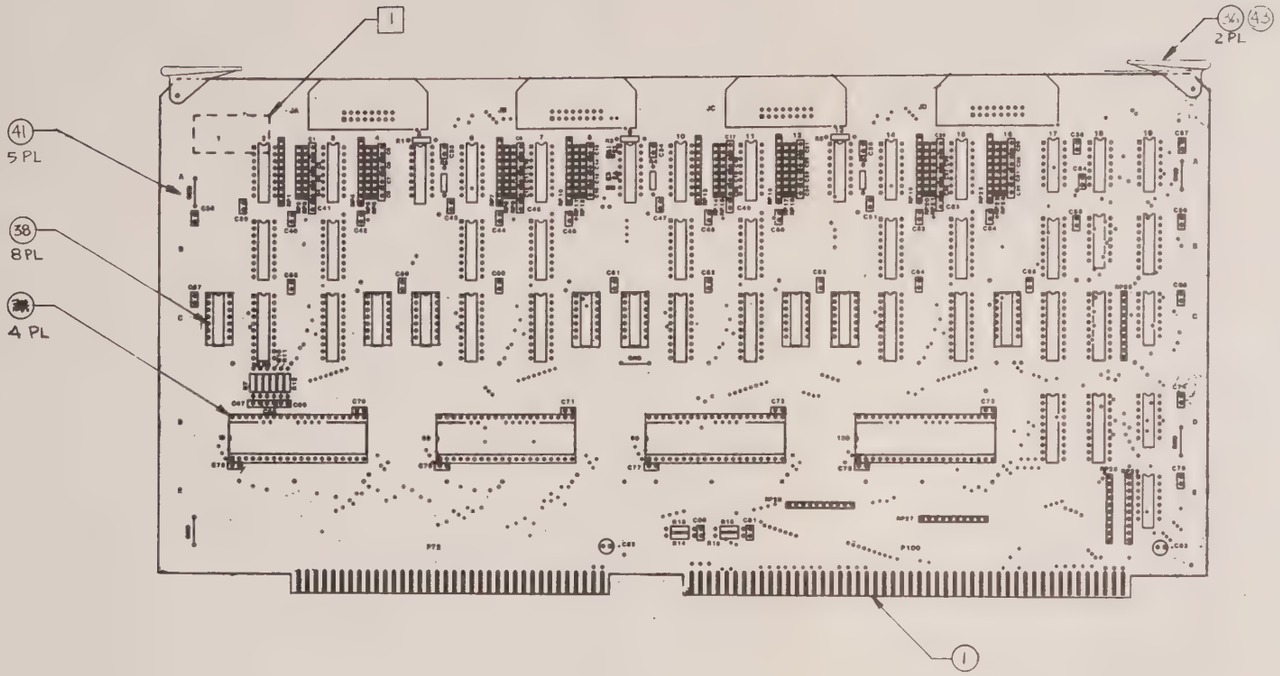
SCALE	SIZE	PART NUMBER	REV
	D	0117-0076	A

CODE

SHEET 7 OF 7

0117-0145 | 1 | A

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	-	-	SEE HISTORY	MW		
	A	[illegible]	PRODUCTION REV	MW	[illegible]	[illegible]



COMPONENT SIDE

NOTES: UNLESS OTHERWISE SPECIFIED.

1. MARK ASSEMBLY DASH NO., REVISION LEVEL AND SERIAL NO. APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK.

2. ASSEMBLY REFLECTS SCHEMATIC DRAWING 0117-0146, AND FABRICATION DRAWING 0117-0147.

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010 — ANGLES: ± 1°

HOLE SIZE: 0.599 ± .003, 600.999 ± .004, 1.000 1.499 ± .005

DRAWN	[illegible]	DATE 2-24-83
CHECKED	[illegible]	5/13/83
PROJ. ENG.	[illegible]	5/13/83
MANUFACTURING	[illegible]	5/13/83
QUALITY ASSUR.	[illegible]	5/13/83

DASH NO	NUMBER	QTY
-10	0117-3200	1
	NEXT ASSEMBLY	

ENG SERV | DATE

GOULD Instruments Division Santa Clara Operations

TITLE: ASSEMBLY, DATA/M-MEMORY (W. GATE ARRAY)

SCALE	SIZE	PART NUMBER	REV
1/1	D	0117-0145	A

MODEL K105 | SHEET 1 OF 1

ITEM	QUANTITY PER ASSEMBLY -45	-40	-35	-30	-25	-20	-15	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	0117-0147-10	P.C. B. DATA, (W. GATE ARRAY)		
2									REF	0117-0146-10	SCHEMATIC - DATA, (W. G. ARRAY)		
3									1	0117-0145-05	PC BOARD		
4								4		0117-0100-10	GATE ARRAY	1D, 5D, 9D, 13D	
5													
6									1	1800-0031-10	I.C. 74S00	18B	
7									1	1800-0060-10	I.C. 74S10	17A	
8									1	1800-0106-10	I.C. 74LS02	19A	
3									1	1800-0110-10	I.C. 74LS10	19E	
10									1	1800-0117-10	I C. 74LS86	19C	
11									1	1800-0123-10	I C 74LS14	19D	
12									1	1800-0237-10	I.C 74LS139	19B	
13									6	1800-0240-10	I C. 74LS244	3C, 7C, 11C, 15C, 18C, 17D	
14									1	1800-0275-10	I C. 74LS21	18A	
15									1	1800-0298-10	I.C 74LS373	18D	
16									9	*1800-0350-10	I C 2'49-45	2B, 3B, 6B, 7B, 10B, 11B, 14B, 15B, 17B	
17									5	1800-0525-10	I.C 74F244	2C, 6C, 10C, 14C, 17C	
18									3	1800-0526-10	I.C 74F161	5A, 9A, 13A	
19									8	1850-0014-10	I C 10125	2A, 3A, 6A, 7A, 10A, 11A, 14A, 15A,	
20								8		9000-0191-10	DELAY LINE	1C, 4C, 5C, 8C, 9C, 12C, 13C, 16C	
21									5	3000-2700-10	RES 270Ω, 1/4W, 5%, CAR.	R7, R9, R11, R14, R16	
22									5	3000-1001-10	RES 1K, 1/4W, 5%, CAR.	R8, R10, R12, R13, R15	
23									6	3000-4701-10	RES 4.7K, 1/4W, 5%,	R1-R6	
24									1	3700-0075-10	RPAK 4.7K 10 PIN	RP25	
25									4	3700-0049-10	RPAK 3K/6.2K 10PIN	RP26-RP29	
26									8	3700-0072-10	RPAK 470 10PIN	RP1, RP4, RP7, RP10, RP13, RP16, RP19, RP22	
27													

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL EC 3992	12/14	MW	RW
=	SEE HISTORY			

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-10	0117-0003	1

	DATE
DWN M. Wolfe	8/31/83
CHK	
ENGR	
MFG.	
Q.A.	

LIST OF MATERIAL
DATA M/M-MEMORY
(W. GATE ARRAY)

GOULD biomation

B | 0117-0145 | REV A

MODEL 105 | SHEET 1 OF 2

KLINGLER K-VEL M10

ITEM	QUANTITY PER ASSEMBLY -45	-40	-35	-30	-25	-20	-15	-10	-05	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
28													
29									16	3700-0117-10	RPAK 68 8PIN	RP2, RP3, RP5, RP6, RP8, RP9, RP11, RP12,	
30												RP14, RP15, RP17, RP18, RP20, RP21, RP23, RP24	
31									81	4010-0103-10	CAP .01UF 100V	C1-C81	
32									2	4400-0043-10	CAP 47UF 6V	C82, C83	
33									1	4010-0101-10	CAP 100PF	C84	
34									4	6100-0143-10	SKT 40 PIN	X1D, X5D, X9D, X13D	
35													
36									2	7000-0120-10	CARD EJECT.		
37													
38									8	6100-0044-10	I C SOCKET	X1C, X4C, X5C, X8C, X9C, X12C, X13C, X16C	
39									4	6000-0374-10	CONN 16 PIN RT. ANG.	JA, JB, JC, JD	
40													
41									5	7000-0359-10	BUSS WIRE FORMED		
42													
43									2	7000-0412-10	CARD EJECTOR PIN		

* NOTE: 1800-0521-10 MAY BE USED IN PLACE OF 1800-0350-10 WHEN NEEDED.

NOTES

LIST OF MATERIAL
DATA M/-MEMORY
(W. GATE ARRAY)

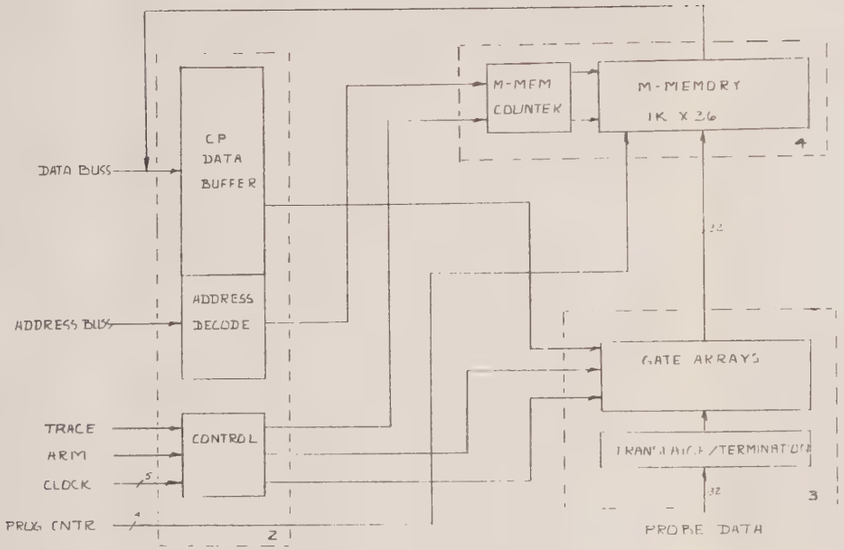
GOULD biomation

B | 0117 0145 | REV A

MODEL K105 | SHEET 2 OF 2

KLINGLER K-VEL M10

REVISIONS						
ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	–	–	SEE HISTORY			
	A	4392	PRODUCTION REL.	MW		



-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: 0 599 = .003; 600 999 = .004; 1 000 1 499 = .005

DRAWN	DATE
CHECKED K Wood	5/12/82
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR.	
ENG. SERV.	DATE

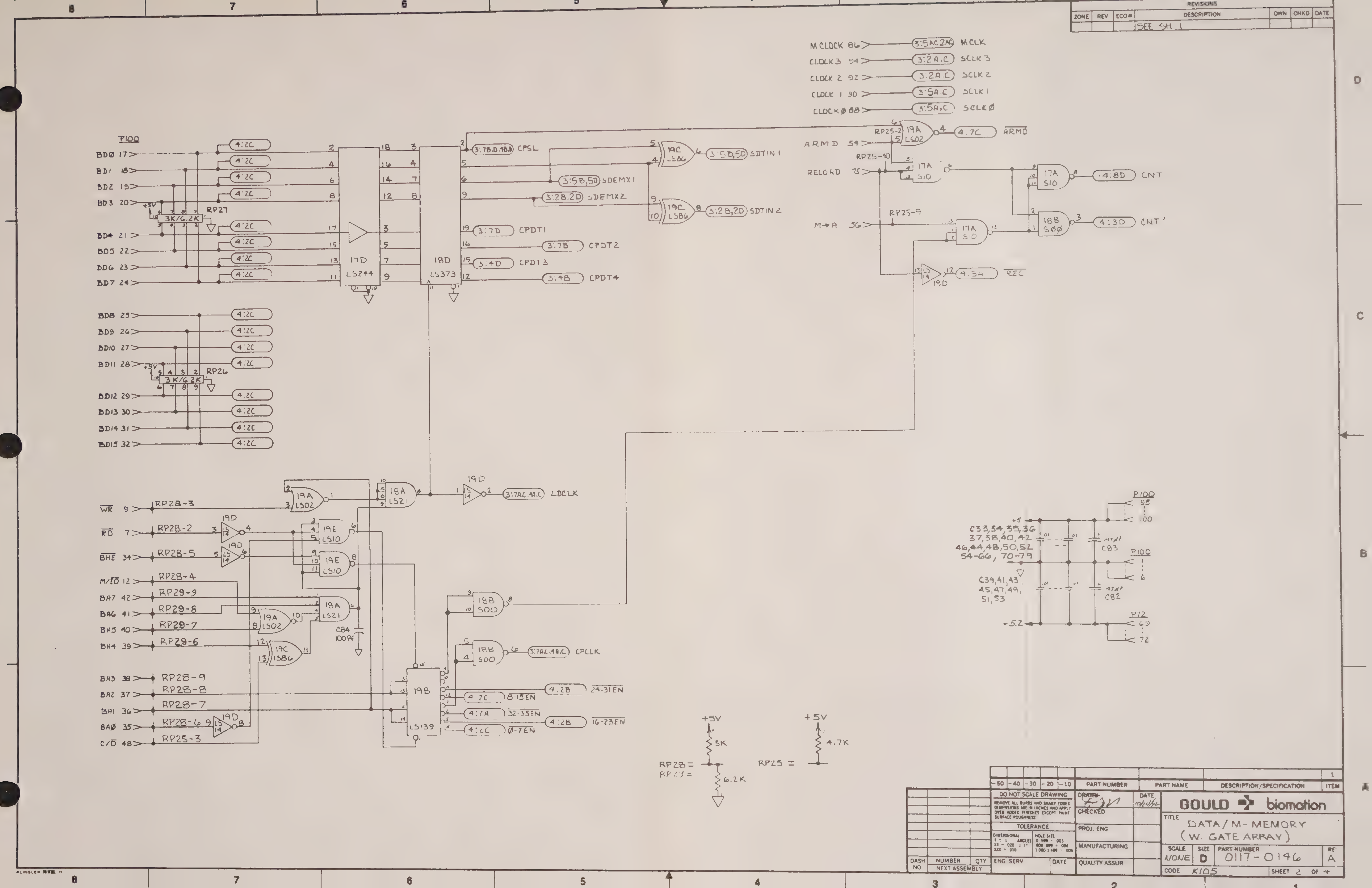
GOULD Instruments Division Santa Clara Operations

TITLE: DATA / M-MEMORY (W. GATE ARRAY)

SCALE	SIZE	PART NUMBER	REV
	D	0117-0146	A

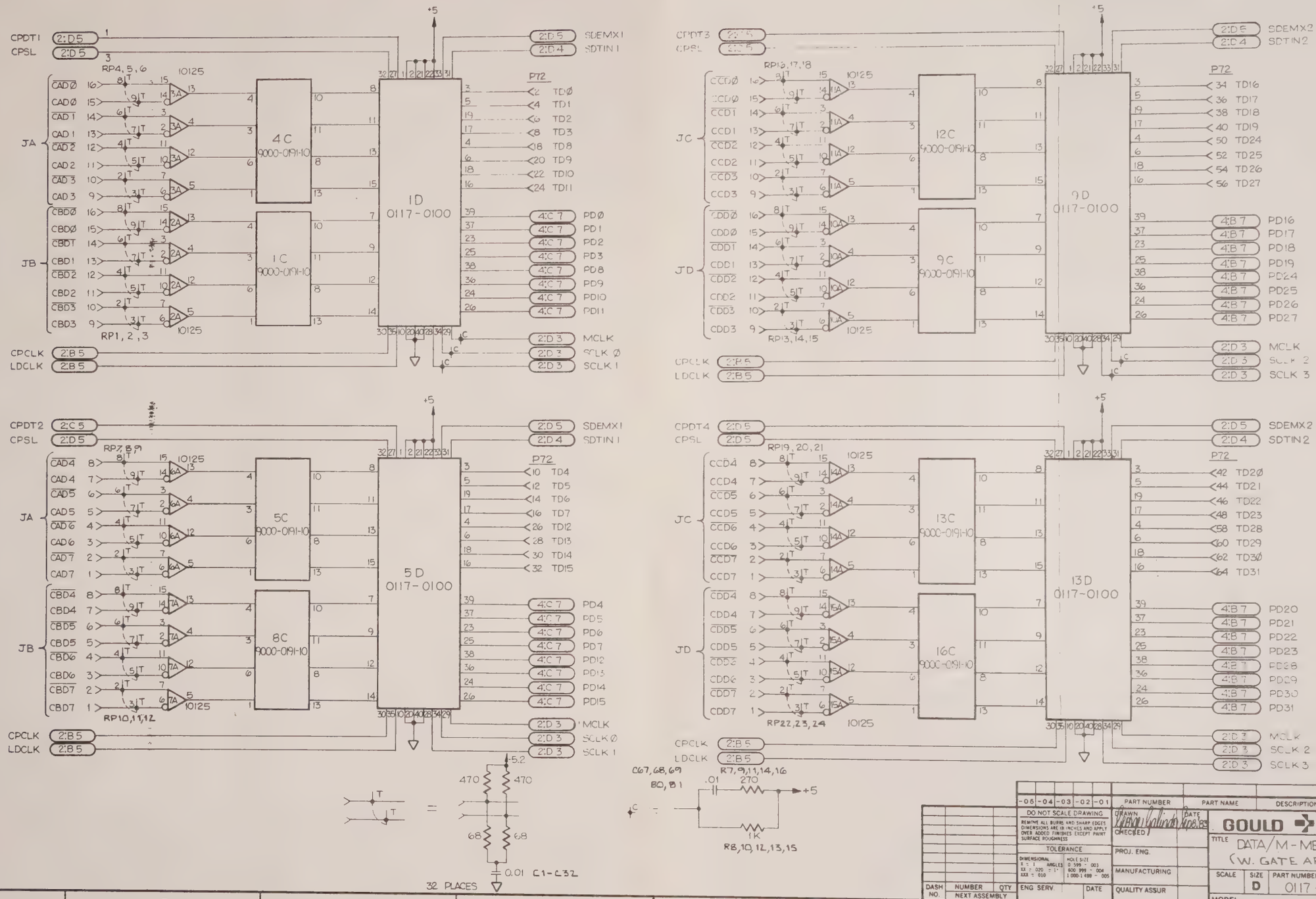
MODEL K 1C5 SHEET 1 OF 9

DASH NO	NUMBER NEXT ASSEMBLY	QTY
-10	0117-0003	1



REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
SEE SH 1
MCLOCK 86 3:5AC,2A MCLK
CLOCK3 94 3:2A,C SCLK3
CLOCK2 92 3:2A,C SCLK2
CLOCK1 90 3:5A,C SCLK1
CLOCKØ 88 3:5A,C SCLKØ
P100
BDØ 17
BD1 18
BD2 19
BD3 20
BD4 21
BD5 22
BD6 23
BD7 24
BD8 25
BD9 26
BD10 27
BD11 28
BD12 29
BD13 30
BD14 31
BD15 32
4:2C
RP27
RP26
3K/6.2K
+5V
17D LS244
18D LS373
3:7B,D,4B,D CPSL
3:5B,5D SDEMX1
3:2B,2D SDEMX2
3:7D CPDT1
3:7B CPDT2
3:4D CPDT3
3:4B CPDT4
19C LS86
3:5D,5D SDTIN1
3:2B,2D SDTIN2
ARMD 54
RP25-2
RP25-10
19A LS02
4.7C ARMD
RECORD 75
17A S10
4:8D CNT
M→A 56
RP25-9
18B SØØ
4:3D CNT'
19D
4.3H REC
WR 9 RP28-3
RD 7 RP28-2
BHE 34 RP28-5
M/IO 12 RP28-4
BA7 42 RP29-9
BA6 41 RP29-8
BA5 40 RP29-7
BA4 39 RP29-6
BA3 38 RP28-9
BA2 37 RP28-8
BA1 36 RP28-7
BAØ 35 RP28-6
C/D 48 RP25-3
19A LS02
18A LS21
3:7A,4A,C LDCLK
19E LS10
C84 100PF
18B S00
3:7A,4A,C CPCLK
19B LS139
4:2C 8-15EN
4:2A 32-35EN
4:2C Ø-7EN
4:2B 24-31EN
4:2B 16-23EN
+5V
3K
RP28 =
RP29 =
6.2K
RP25 =
4.7K
C33,34,35,36
37,38,40,42
46,44,48,50,52
54-66, 70-79
C39,41,43,
45,47,49,
51,53
C83
C82
47μf
+5
-5.2
P100
95
100
P72
69
72
DO NOT SCALE DRAWING
TOLERANCE
DASH NO | NUMBER | QTY
NEXT ASSEMBLY
ENG SERV | DATE
PART NUMBER | PART NAME | DESCRIPTION/SPECIFICATION | ITEM
DRAWN
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE DATA / M-MEMORY (W. GATE ARRAY)
SCALE NONE
SIZE D
PART NUMBER 0117-0146
REV A
CODE KIOS
SHEET 2 OF 4

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SH 1			



DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 = 1°; XXX = .010

HOLE SIZE: 0.599 - .003; 600 999 - .004; 1.000-1.499 - .005

ENG SERV. | DATE

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
-05-04-03-02-01			1

DRAWN | DATE

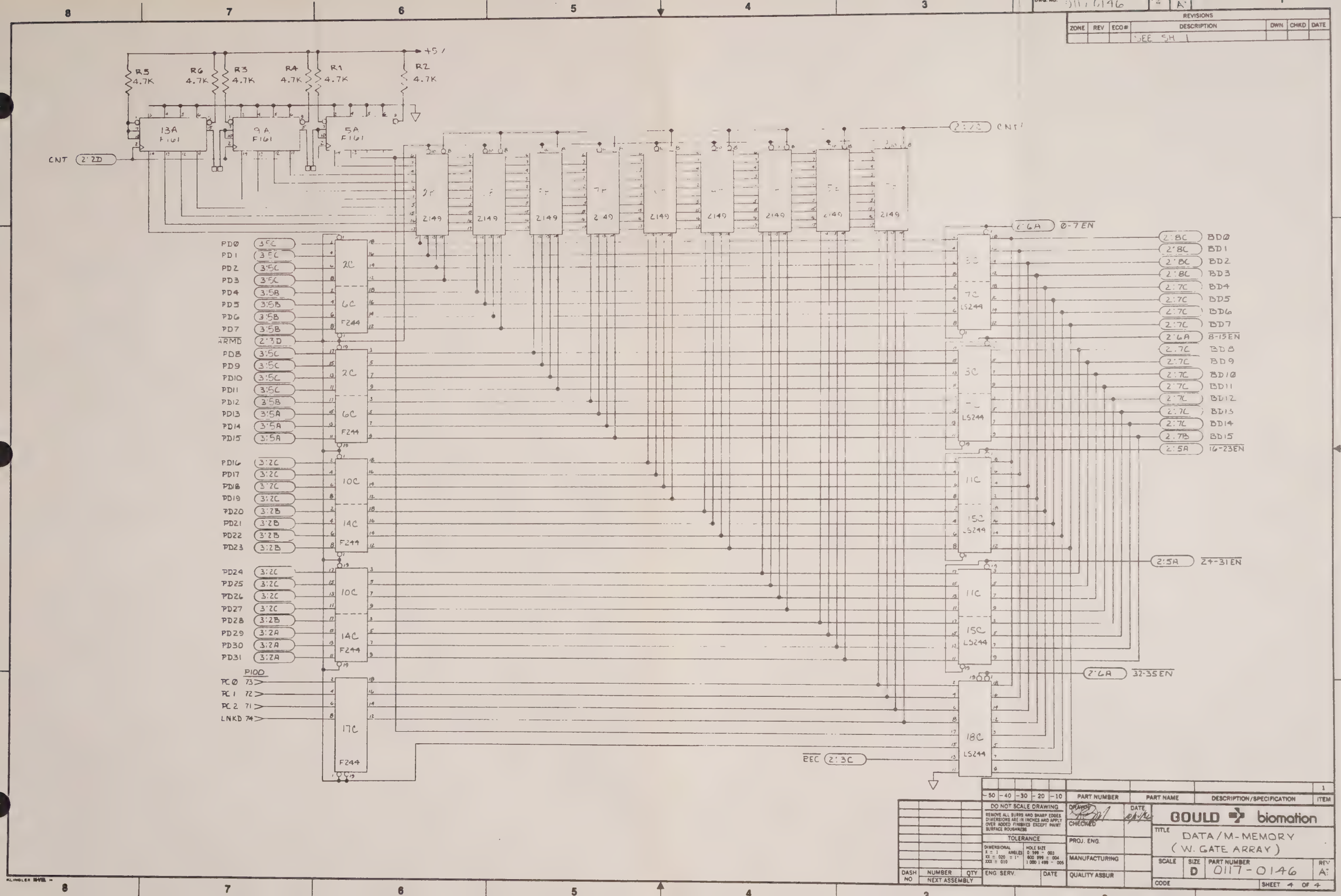
CHECKED

GOULD Instruments Division Santa Clara Operations

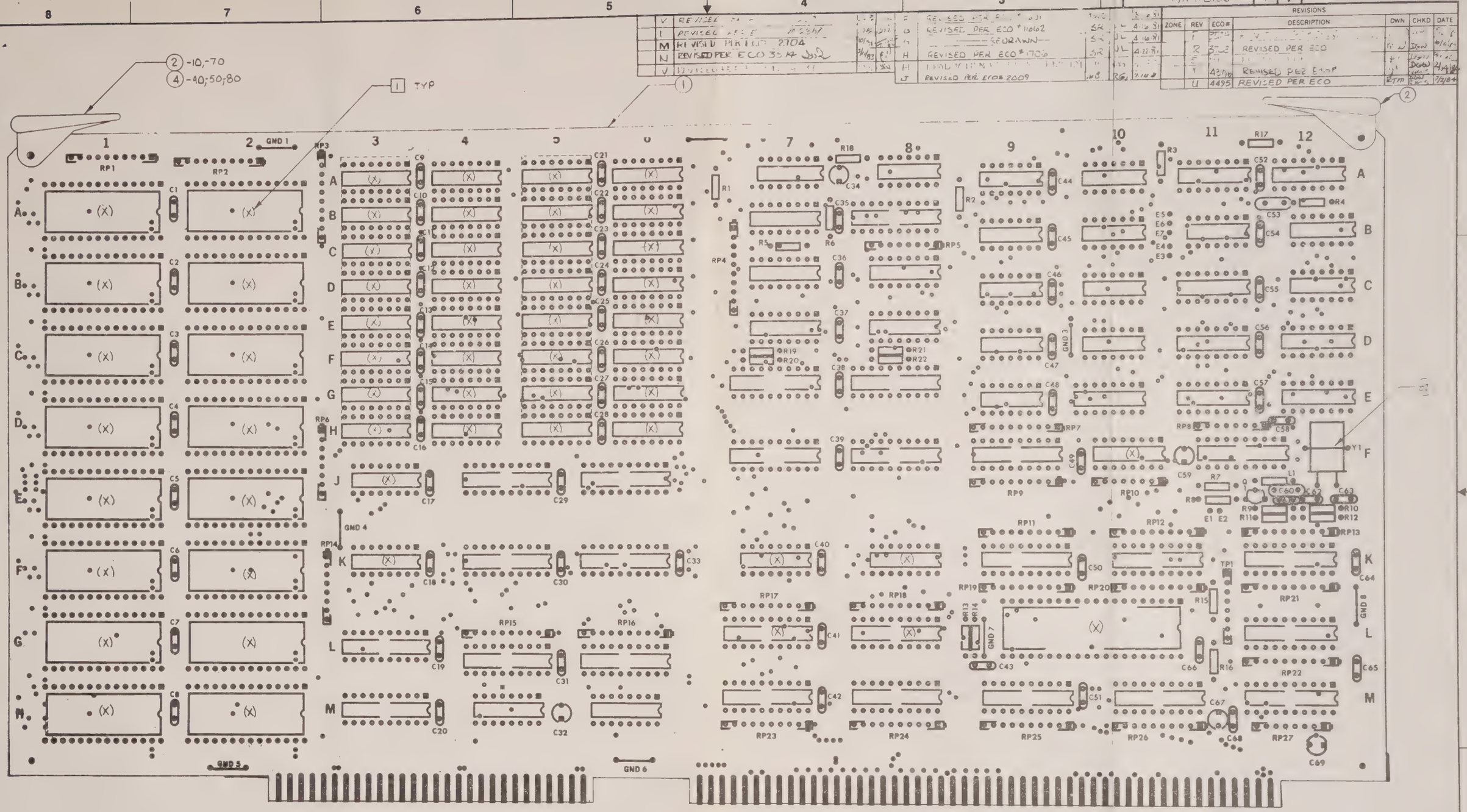
TITLE: DATA/M-MEMORY (W. GATE ARRAY)

SCALE	SIZE	PART NUMBER	REV
	D	0117-0146	A

MODEL | SHEET 3 OF 4



REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SH 1
+5V
R5 4.7K
R6 4.7K
R3 4.7K
R4 4.7K
R1 4.7K
R2 4.7K
13A F161
9A F161
5A F161
CNT 2:2D
2:2C CNT
2149
2C 6C F244
10C 14C F244
17C F244
3C 7C LS244
11C 15C LS244
18C LS244
PD0 3:5C
PD1 3:5C
PD2 3:5C
PD3 3:5C
PD4 3:5B
PD5 3:5B
PD6 3:5B
PD7 3:5B
ARMD 2:3D
PD8 3:5C
PD9 3:5C
PD10 3:5C
PD11 3:5C
PD12 3:5B
PD13 3:5A
PD14 3:5A
PD15 3:5A
PD16 3:2C
PD17 3:2C
PD18 3:2C
PD19 3:2C
PD20 3:2B
PD21 3:2B
PD22 3:2B
PD23 3:2B
PD24 3:2C
PD25 3:2C
PD26 3:2C
PD27 3:2C
PD28 3:2B
PD29 3:2A
PD30 3:2A
PD31 3:2A
P100
PC0 73
PC1 72
PC2 71
LNKD 74
2:6A 0-7EN
2:8C BD0
2:8C BD1
2:8C BD2
2:8C BD3
2:7C BD4
2:7C BD5
2:7C BD6
2:7C BD7
2:6A 8-15EN
2:7C BD8
2:7C BD9
2:7C BD10
2:7C BD11
2:7C BD12
2:7C BD13
2:7C BD14
2:7B BD15
2:5A 16-23EN
2:5A 24-31EN
2:6A 32-35EN
EEC 2:3C
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DASH NO NUMBER QTY
NEXT ASSEMBLY
ENG SERV. DATE
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
DRAWN CHECKED PROJ. ENG. MANUFACTURING QUALITY ASSUR
GOULD biomation
TITLE DATA/M-MEMORY (W. GATE ARRAY)
SCALE SIZE D PART NUMBER 0117-0146 REV A
CODE SHEET 4 OF 4



COMPONENT SIDE

NOTES:

1. THIS SYMBOL (X) INDICATES WHERE I.C. SOCKETS ARE REQUIRED (FOR REF ONLY)

DASH NO	NUMBER	QTY
-50	0114-0002	1
-40	0114-0002	1
-30	0114-0073	1
-20	0114-0002	1
-10	0950-0002	1

NEXT ASSEMBLY

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°; HOLE SIZE: 0.599 - .003, 600.999 - .004, 1.000 1.499 - .005

ENG. SERV. RG DATE 5/29/81

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DRAWN S. Rodell DATE 4-16-81

CHECKED RG 5/29/81

PROJ ENG

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: ASSEMBLY, K101, K500 MPU BD.

SCALE 2:1 | SIZE D | PART NUMBER 0114-0185 | REV V

CODE K101, K500 | SHEET 1 OF 1

GOULD

TITLE			DRAWING NO.	REV
ASSEMBLY MPU PWB	LM		0114-0185	V
DWN JW 2-9-84	CHK DCW	ENG	MFG	MODEL K101, K102 K500	SHEET 1 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
1.	0114-0187	1	–			–		MPU P.C. BOARD	
2.	7000-0120	–	2			1		EJECTOR	LEFT SIDE (A11) (& RIGHT ON -10,-70)
3.	0114-0185-05	–	1			1		MPU BOARD SUB ASSEMBLY	
4.	0112-0228-07	–	–			1		EJECTOR, STAMPED A7	RIGHT SIDE (A12)
5.									
6.									
7.	0950-0191	–	1			–		I.C.	10F ROM, ADD. MAP
8.	0950-0193	–	1			–			3J ROM, CHIP SEL
9.	0950-0192	–	1			–			3K ROM. CHIP SEL
10.									
11.	0114-0066	–	–			1			10F ROM ADD. MAP
12.	0114-0067	–	–			1			3J ROM, CHIP SEL
13	0114-0069	–	–			1			3K ROM, CHIP SEL
14.									
15.	1800-0321	–	1			1		I.C.	10L 8086
16.	0117-0017-01	–	–			–		I.C, ROM ADD MAP	10F

REV	ECO	CHK	APPD	DATE
T	4306		JMS	4-4-84
U	4484	DCW	JMS	7/10/84
V	4587		JWC	

NOTES:

DASH #	NEXT ASSY	QTY
-10	0950-0002	1
-20	0114-0002	1
-30	0114-0073	1
-40	0114-0002	1
-50	0114-0002	1

GOULD

TITLE			DRAWING NO.	REV
ASSEMBLY MPU PWB	LM		0114-0185	V
DWN JW 2-9-84	CHK DCW	ENG	MFG	MODEL	SHEET 2 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-90	U/M	DESCRIPTION	REFERENCE DESIGNATION
1.	0114-0187	–		–	–			P.C. BOARD	
2.	7000-0120	1		2	1			EJECTOR	
3.	0114-0185-05	1		1	1			MPU BOARD SUBASSEMBLY	
4.	0112-0228-07	1		–	1			EJECTOR STAMPED A7	
5									
6.									
7.	0950-0191	–		–	–			I.C.	10F ROM ADD MAP
8.	0950-0193	–		–	–				3J ROM CHIP SEL
9.	0950-0192	–		–	–				3K ROM CHIP SEL
10.									
11.	0114-0066	1		–	1				10F ROM ADD MAP
12.	0114-0067	1		–	1				3J ROM CHIP SEL
13.	0114-0069	1		–	1				3K ROM CHIP SEL
14.									
15	1800-0321	1		1	1			I.C.	10L 8086
16.	0117-0017-01	–		1	–			I.C. ROM ADD MAP	10F

REV	ECO	CHK	APPD	DATE

NOTES: BASIC -05 SUBASSEMBLY
-10: K500 -20: N/A -30 N/A
-40: K101 WITH STORAGE
-50: K102 WITH STORAGE -60: N/A
-70: K105 -80: K205

DASH #	NEXT ASSY	QTY

GOULD

TITLE	LM	DRAWING NO.	REV
ASSEMBLY MPU PWB		0114-0185	V
	MODEL	SHEET 3 OF 12	

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
17.	0117-0018-01	—	—			—		I.C., ROM CHIP SEL	3J
18.	0117-0019-01	—	—			—		I.C., ROM CHIP SEL	3K
19.									
20.	1800-0353	—	—			32		I.C. 4164, 64K RAM	3A-3H, 5A-5H, 4A-4H, 6A-6H
21.	6100-0120	37	—			—		SOCKET, 16 PIN DIP, LP	X3J, X3K, X7K, X8K, X10F, X3A-X3H, X4A-X4H, X5A-X5H, X6A-X6H
22.									
23.	1400-0019	1	—			—		TRANSISTOR 2N3906	Q1
24.									
25.	1800-0031	3	—			—		I.C. 74S00, 14	9B, 10B, 12B
26.	1800-0038	1	—			—		74S20	9C
27.	1800-0039	8	—			—		74S112	10E, 11A, 11C, 11D, 11E, 12A, 12D, 12E
28.	1800-0060	4	—			—		74S10	7A, 8A, 9D, 12C
29.	1800-0092	1	—			—		74S04	10A
30.	1800-0107	1	—			—		74LS04	9E
31.	1800-0125	4	—			—		74LS161	7C, 7D, 8C, 8D
32.	1800-0133	1	—			—		74S11	10C
33.	1800-0136	1	—			—		74S51	10D
34.	1800-0208	1	—			—		74S161	7B
35.	1800-0240	9	—			—		74LS244	3L, 3M, 4J, 6J, 7E, 7F, 8E, 8F, 9F
36.	1800-0243	2	—			—		I.C. 74S08	9A, 11B

GOULD

TITLE	LM	DRAWING NO.	REV
ASSEMBLY MPU PWB		0114-0185	V
	MODEL	SHEET 4 OF 12	

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-	U/M	DESCRIPTION	REFERENCE DESIGNATION
17.	0117-0018-01	—		1	—			I.C. ROM CHIP SEL	
18.	0117-0019-01	—		1	—			I.C. ROM CHIP SEL	
19.									
20.	1800-0353	32		32	32			I.C. 4164, 64K RAM	
21.	6100-0120	—		—	—			SOCKET, 16PIN DIP, LP	
22.									
23.	1400-0019	—		—	—			TRANSISTOR, 2N3906	
24.									
25.	1800-0031	—		—	—			I.C. 74S00	
26.	1800-0038	—		—	—			74S20	
27.	1800-0039	—		—	—			74S112	
28.	1800-0060	—		—	—			74S10	
29.	1800-0092	—		—	—			74S04	
30.	1800-0107	—		—	—			74LS04	
31.	1800-0125	—		—	—			74LS161	
32.	1800-0133	—		—	—			74S11	
33.	1800-0136	—		—	—			74S51	
34.	1800-0208	—		—	—			74S161	
35.	1800-0240	—		—	—			74LS244	
36.	1800-0243	—		—	—			I.C. 74S08	

GOULD

TITLE	LM	DRAWING NO.	REV
ASSEMBLY MPU PWB		0114-0185	V
	MODEL	SHEET 5	OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
37.	1800-0268	2	–			–		I.C. 74LS245	7M, 8M
38.	1800-0298	10	–			–		I.C. 74LS373	4K,4L,6K,6L,9K,9M,10K,10M,11K,11L
39.	1800-0320	–	16			–		I.C. 2118 RAM	4A-4H, 6A-6H
40.	1800-0335	2	–			–		I.C. 74LS166	4M, 6M
41.	1800-0353	–	–			–		IC	4A-4H, 6A-H
42.	1800-0261	3	–			–		I.C. 74S240	8B. 11F, 11M
43.	2100-0009	1	–			–		INDUCTOR 1.5uH	L1
44.									
45.									
46.	3000-1000	1	–			–		RESISTOR, 100Ω, 1/4W, 5%	R11
47.	3000-1300	1	–			–		130Ω	R9
48.	3000-1601	2	–			–		1.6K	R6, 10
49.	3000-2006	1	–			–		20Ω	R4
50.	3000-2200	3	–			–		220	R7, 19, 21
51.	3000-2201	7	–			–		2.2K	R1-3, 5, 15, 17, 18
52	3000-2700	1	–			–		270Ω	R13
53	3000-3300	3	–			–		330Ω	R8, 20, 22
54	3000-3301	1	–			–		3.3K	R12
55	3000-5100	1	–			–		510Ω	R16
56	3000-9106	1	–			–		91Ω 1/4W 5%	R14

GOULD

TITLE	LM	DRAWING NO.	REV
ASSEMBLY MPU PWB		0114-0185	V
	MODEL	SHEET 6	OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-	U/M	DESCRIPTION	REFERENCE DESIGNATION
37.	1800-0268	–		–	–			I.C. 74LS245	
38.	1800-0298	–		–	–			IC. 74LS373	
39.	1800-0320	–		–	–			I.C. 2118 RAM	
40.	1800-0335	–		–	–			I.C. 74LS166	
41.	1800-0353	–		–	–			I.C.	
42.	1800-0261	–		–	–			IC. 74S240	
43.	2100-1000	–		–	–			INDUCTOR 1.5uH	
44.									
45.									
46.	3000-1000	–		–	–			RESISTOR 100Ω, 1/4W, 5%	
47.	3000-1300	–		–	–			130Ω	
48.	3000-1601	–		–	–			1.6K	
49.	3000-2006	–		–	–			20Ω	
50.	3000-2200	–		–	–			220Ω	
51.	3000-2201	–		–	–			2.2K	
52.	3000-2700	–		–	–			270Ω	
53.	3000-3300	–		–	–			330Ω	
54.	3000-3301	–		–	–			3.3K	
55.	3000-5100	–		–	–			510Ω	
56.	3000-9106	–		–	–			RESISTOR 91Ω	

GOULD

TITLE		DRAWING NO.	REV
ASSEMBLY MPU PWB	LM	0114-0185	V
	MODEL	SHEET 7	OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
57.	3700-0049	13	–			–		RES. PAK, 3K/6.2K, 10 PIN SIP	RP1, 2, 7, 9, 15-18, 22-26
58.	3700-0057	6	–			–		RES. PAK, 2.2K, 8 PIN SIP	RP5, 6, 8, 10, 14, 27
59.	3700-0065	5	–			–		RES. PAK, 220/330, 10 PIN SIP	RP3, 4, 11-13
60.	3700-0066	3	–			–		RES. PAK, 10K, 10 PIN SIP	RP19-21
61.									
62.									
63.	4000-0040	1	–			–		CAP. 470pf	C43
64.	4000-0044	61	–			1		CAP. .01uf, ±20%, 100V	C1-31, 33, 35-42, 54-58, 61-66, 68, 44-52, 67
65.									
66.									
67.	4100-0019	1	–			–		CAP. 50pf	C53
68	4100-0029	1	–			–		CAP. 30pf	C60
69.									
70.	4400-0043	4	1			–		CAP. 47uf, ±10%, 6V	C32, 34, 59, 67, 69
71									
72.	5100-0016	1	–			–		CRYSTAL, 24MHZ	Y1
73.									
74.	6000-0190	1	–			–		HEADER, 8 PIN CONN	TP1
75.									
76.									

GOULD

TITLE		DRAWING NO.	REV
ASSEMBLY MPU PWB	LM	0114-0185	V
	MODEL	SHEET 8	OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-90	U/M	DESCRIPTION	REFERENCE DESIGNATION
57.	3700-0049	–		–	–			RES. PAK, 3K/6.2K, 10 PIN SIP	
58.	3700-0057	–		–	–			RES. PAK, 2.2K, 8 PIN SIP	
59.	3700-0065	–		–	–			RES. PAK, 220/330, 10 PIN SIP	
60.	3700-0066	–		–	–			RES. PAK, 10K, 10 PIN SIP	
61.									
62.									
63.	4000-0040	–		–	–			CAP. 470pf	
64.	4000-0044	–		–	–			CAP. .01uf, ±20%, 100V	
65.									
66.									
67.	4100-0019	–		–	–			CAP. 50pf	
68.	4100-0029	–		–	–			CAP. 30pf	
69.									
70.	4400-0043	–		–	–			CAP. 47uf, ±10%, 6V	
71.									
72.	5100-0016	–		–	–			CRYSTAL, 24MHZ	
73.									
74.	6000-0190	–		–	–			HEADER, 8 PIN CONN	
75.									
76.									

GOULD

TITLE ASSEMBLY MPU PWB | LM | DRAWING NO. 0114-0185 | REV V

MODEL | SHEET 9 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
77.	6100-0121	2	–			–		SOCKET 20 PIN	X7L, X8L
78.	6100-0123	1	–			–		SOCKET 40 PIN	X10L
79.	6100-0151	16	–			–		SOCKET 28 PIN	X1A-X1H, X2A-X2H
80.									
81.									
82.	7100-0017	.1	–			–		WIRE CRYSTAL STRAP #22AWG	Y1
83.									
84.									
85.	9000-0054	8	–			–		WIRE, FORMED 16 PIN	GND1 - GND8
86.									
87.									
88.	0120-0085-10	–	–			–		ASSY., 16 PROM SET PROGRAM CODE K20S (REF ITEMS 98 TO 113)	
89.	0114-2020-10	–	–			1		ASSY., PROM K101 CODE (REF ITEMS 98 TO 113)	
90.	0114-2021-10	–	–			–		ASSY., PROM K102 CODE (REF ITEMS 98 TO 113)	
91.	0950-0150-10	–	1			–		ASSY., PROM K500 CODE (REF ITEMS 98 TO 113)	
92.									
93.									
94.									
95.									
96.									

GOULD

TITLE ASSEMBLY MPU PWB | LM | DRAWING NO. 0114-0185 | REV V

MODEL | SHEET 10 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-90	U/M	DESCRIPTION	REFERENCE DESIGNATION
77	6100-0121	–		–	–	–		SOCKET 20 PIN	X7L, X8L
78	6100-0123	–		–	–	–		SOCKET 40 PIN	X10L
79	6100-0151	–		–	–	–		SOCKET 28 PIN	X1A-X1H, X2A-X2H
80									
81									
82	7100-0017	–		–	–	–		WIRE, CRYSTAL STRAP, #22AWG	Y1
83									
84									
85	9000-0054	–		–	–	–		WIRE FORMED 16 PIN	GND1-GND8
86									
87									
88	0120-0085-10	–		–	1	–		ASSY 16 PROM SET PROGRAM CODE K20S (REF ITEMS 98 TO 113)	
89	0114-2020-10	–		–	–	–		ASSY PROM K101 CODE (REF ITEMS 98 TO 113)	
90	0114-2021-10	1		–	–	–		ASSY PROM K102 CODE (REF ITEMS 98 TO 113)	
91	0950-0150-10	–		–	–	–		ASSY PROM K500 CODE (REF ITEMS 98 TO 113)	
92									
93									
94									
95									
96									

GOULD

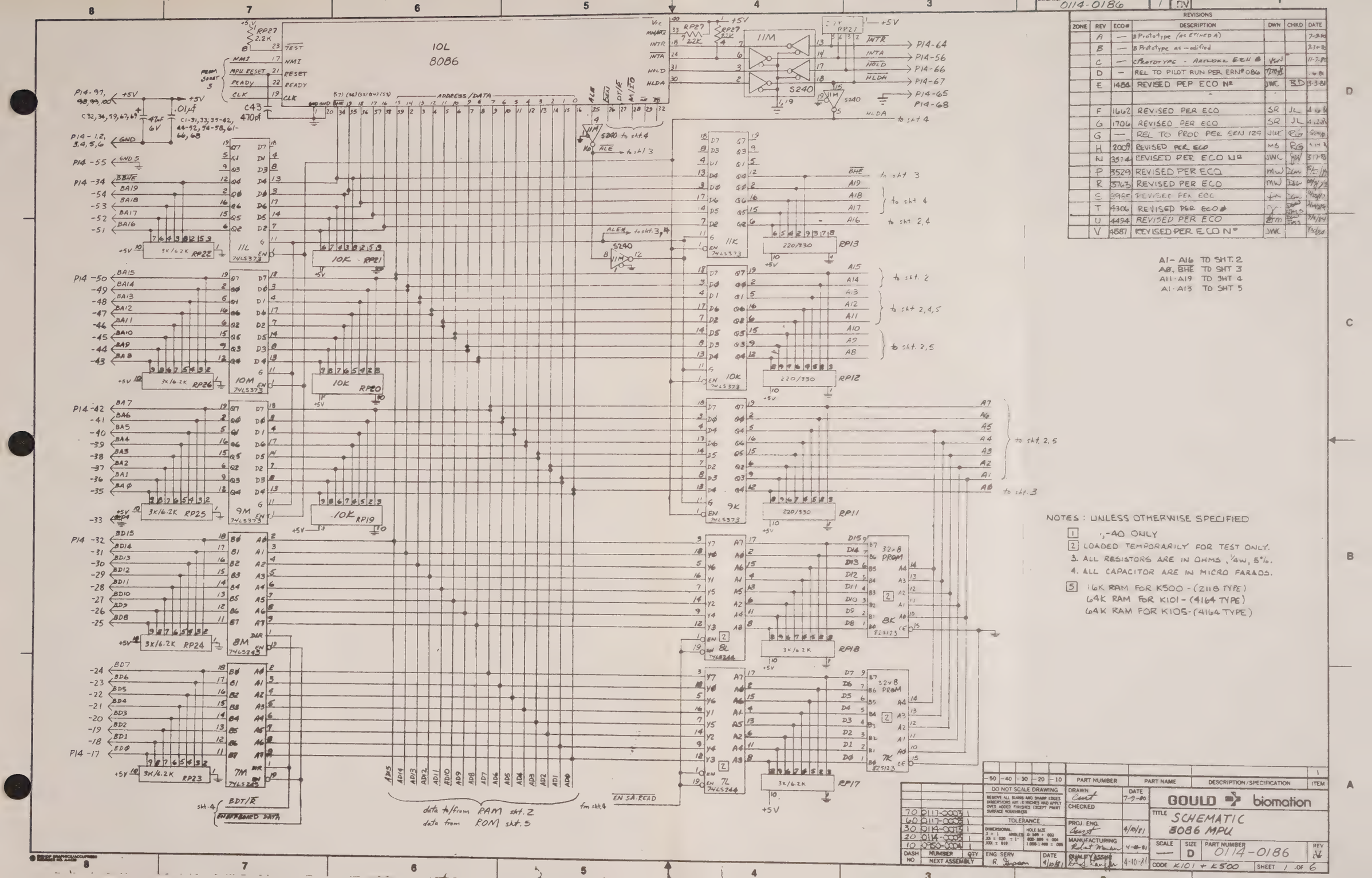
TITLE		DRAWING NO.	REV
ASSEMBLY MPU PWB	LM	0114-0185	V
	MODEL	SHEET 11 OF 12	

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
97.	0117-0020-10	–	–			–		ASSY 16 PROM SET PROGRAM CODE (REF ITEMS 98 TO 112)	
98.	1 OF 16	–	REF			REF		PROGRAMMED PROM	2H
99.	2	–							1H
100.	3	–							2G
101.	4	–							1G
102.	5	–							2F
103.	6	–							1F
104.	7	–							2E
105.	8	–							1E
106.	9	–							2D
107.	10	–							1D
108	11	–							2C
109	12	–							1C
110	13	–							2B
111	14	–							1B
112	15	–							2A
113	16 OF 16	–	REF			REF		PROGRAMMED PROM	1A
114									
115									
116									

GOULD

TITLE		DRAWING NO.	REV
ASSEMBLY MPU PWB	LM	0114-0185	V
	MODEL	SHEET 12 OF 12	

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-	U/M	DESCRIPTION	REFERENCE DESIGNATION
97.	0117-0020-110	–		1	–			ASSY 16 PROM SET PROGRAM CODE (REF ITEMS 98 TO 112)	
98.	1 OF 16	REF		REF	REF			PROGRAMMED PROM	2H
99.	2								1H
100.	3								2G
101.	4								1G
102.	5								2F
103.	6								1F
104.	7								2E
105.	8								1E
106.	9								2D
107.	10								1D
108.	11								2C
109.	12								1C
110.	13								2B
111.	14								1B
112.	15								2A
113.	16 OF 16	REF		REF	REF			PROGRAMMED PROM	1A
114.									
115.									
116.									



REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	—	B Prototype (as ETCHED A)			7-3-80
	B	—	B Prototype as-modified			8-30-80
	C	—	C PROTOTYPE - ARTWORK ERN #	KW		11-7-80
	D	—	REL TO PILOT RUN PER ERN# 0860	KW		1-6-81
	E	1484	REVISED PER ECO N°	JWC	BD	3-3-81
			-			
	F	1662	REVISED PER ECO	SR	JL	4-10-81
	G	1706	REVISED PER ECO	SR	JL	4-28-81
	G	—	REL TO PROD PER ERN 129	JWC	RG	5-6-81
	H	2009	REVISED PER ECO	MS	RG	5-14-81
	N	3514	REVISED PER ECO N°	JWC	KW	8-17-83
	P	3529	REVISED PER ECO	MW	JLW	9-6-83
	R	3763	REVISED PER ECO	MW	JLW	09/4/83
	S	3985	REVISED PER ECO	KW	JLW	09/20/83
	T	4306	REVISED PER ECO #	KW	DMS DMS JLW	2/14/84
	U	4494	REVISED PER ECO	KW	JLW	3/5/84
	V	4587	REVISED PER ECO N°	JWC		4/26/84

A1 - A16 TO SHT. 2
A8, BHE TO SHT 3
A11 - A19 TO SHT 4
A1 - A13 TO SHT 5

NOTES: UNLESS OTHERWISE SPECIFIED

1. -40 ONLY
2. LOADED TEMPORARILY FOR TEST ONLY.
3. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
4. ALL CAPACITOR ARE IN MICRO FARADS.
5. 16K RAM FOR K500 - (2118 TYPE)
   64K RAM FOR K101 - (4164 TYPE)
   64K RAM FOR K105 - (4164 TYPE)

DASH NO	NUMBER	QTY
70	0117-0007	1
60	0117-0008	1
30	0114-0015	1
20	0114-0009	1
10	0060-0004	1

NEXT ASSEMBLY

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL
.X ± .020 ± 1°
.XX ± .010
ANGLES ± 30'
HOLE SIZE
.0-.500 ± .002
.500-.999 ± .004
1.000-1.499 ± .005

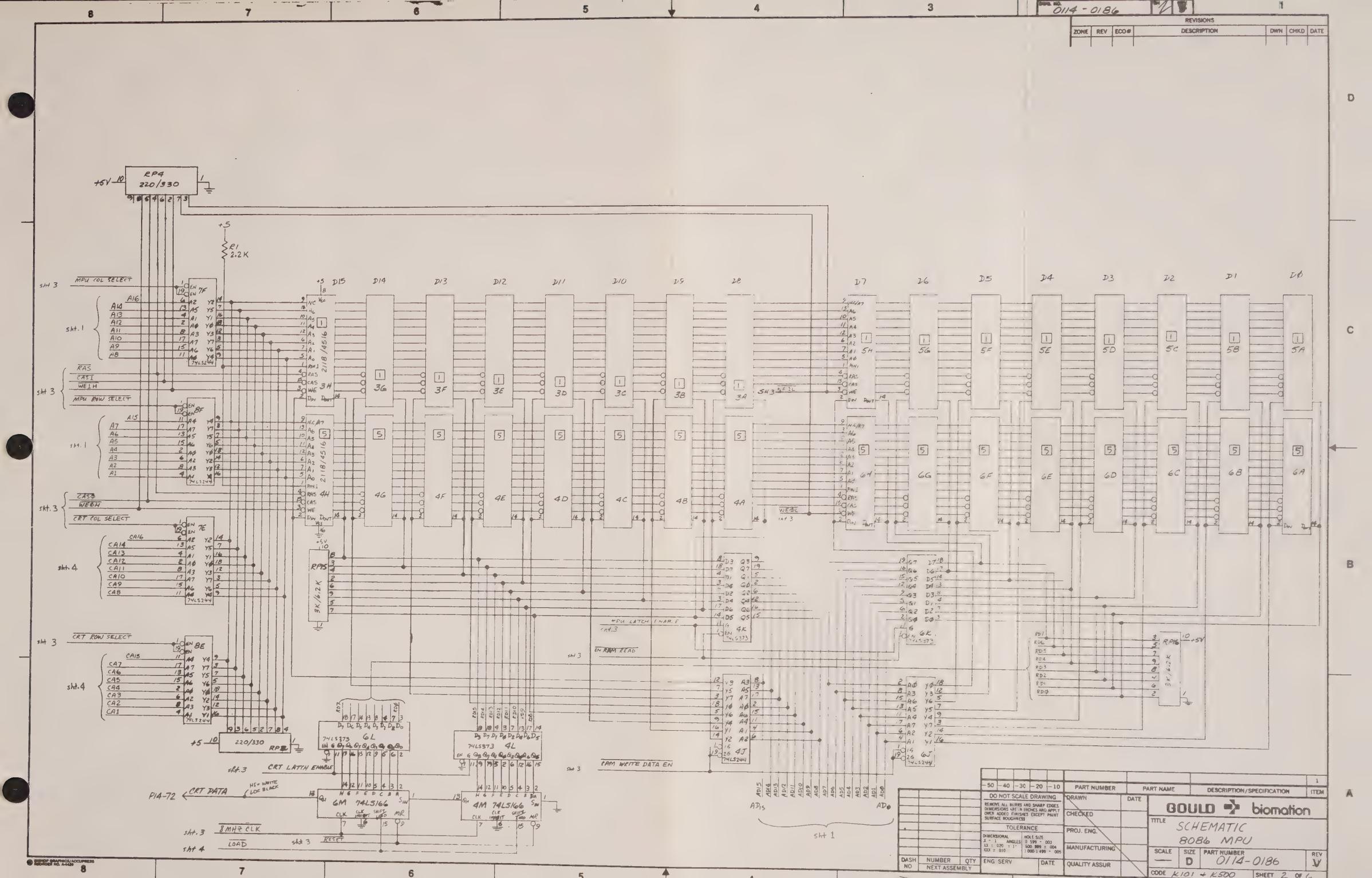
DRAWN	Kent	7-9-80
CHECKED		
PROJ. ENG.	Kent	4/8/81
MANUFACTURING	Robert Mann	4-8-81
ENG SERV	R. Swan	4/8/81
QUALITY ASSUR	Ed Carlin	4-10-81

GOULD biomation

TITLE: SCHEMATIC 8086 MPU

SCALE	SIZE	PART NUMBER	REV
—	D	0114-0186	V

CODE K101 + K500 | SHEET 1 OF 6



REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG SERV DATE

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DRAWN DATE

CHECKED

PROJ. ENG.

MANUFACTURING

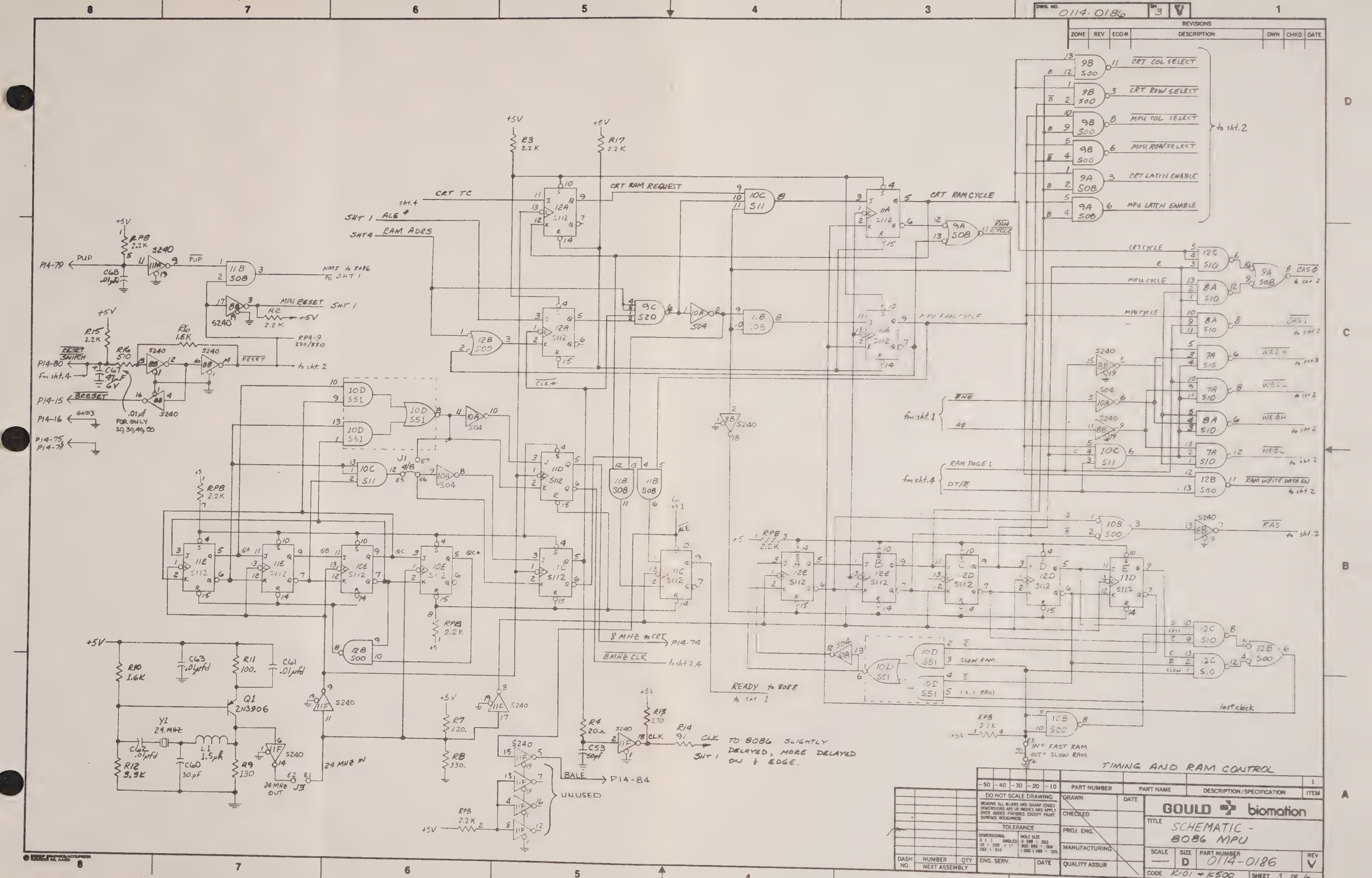
QUALITY ASSUR

GOULD biomation

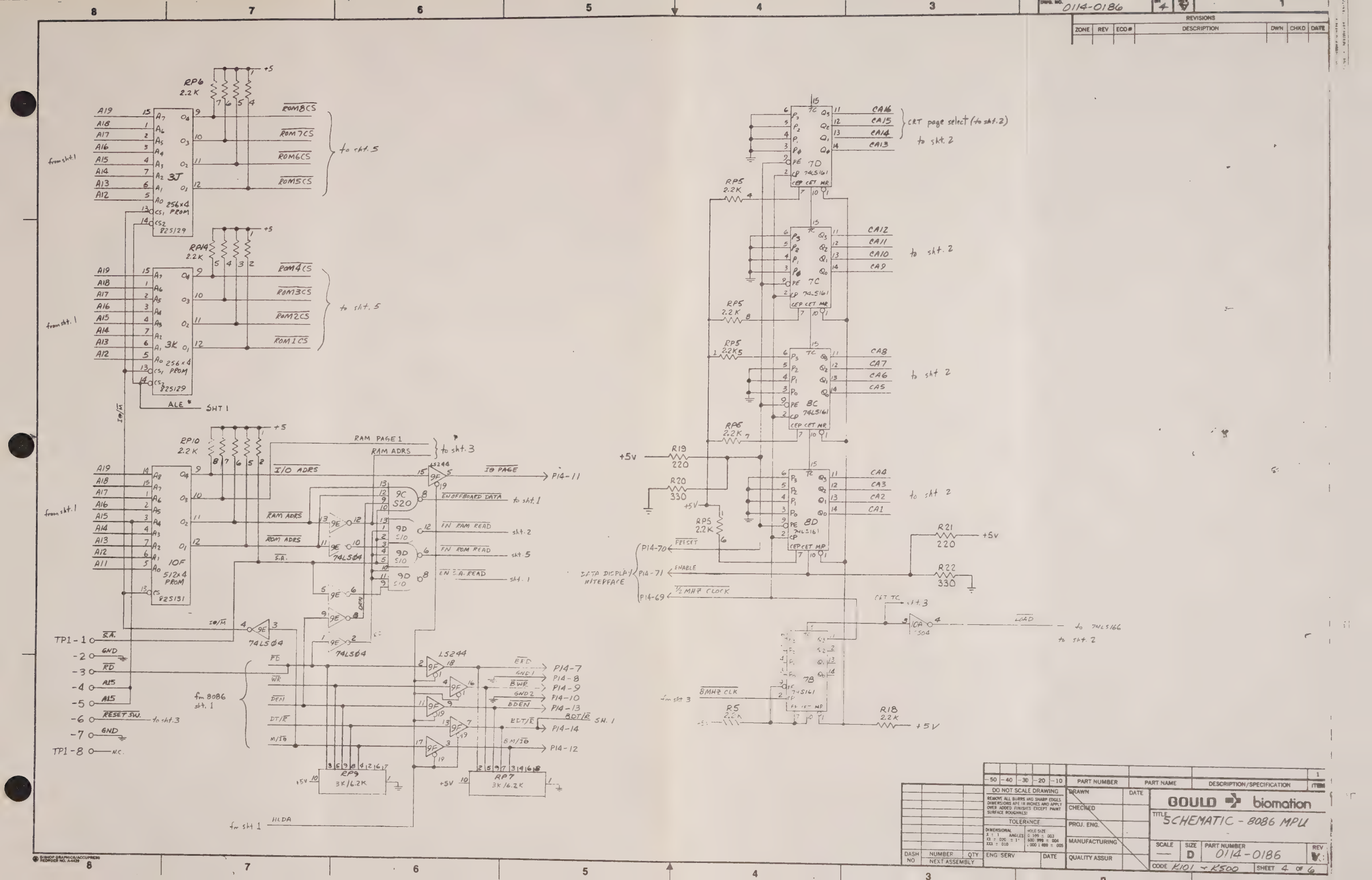
TITLE SCHEMATIC 8086 MPU

SCALE — SIZE D PART NUMBER 0114-0186 REV W

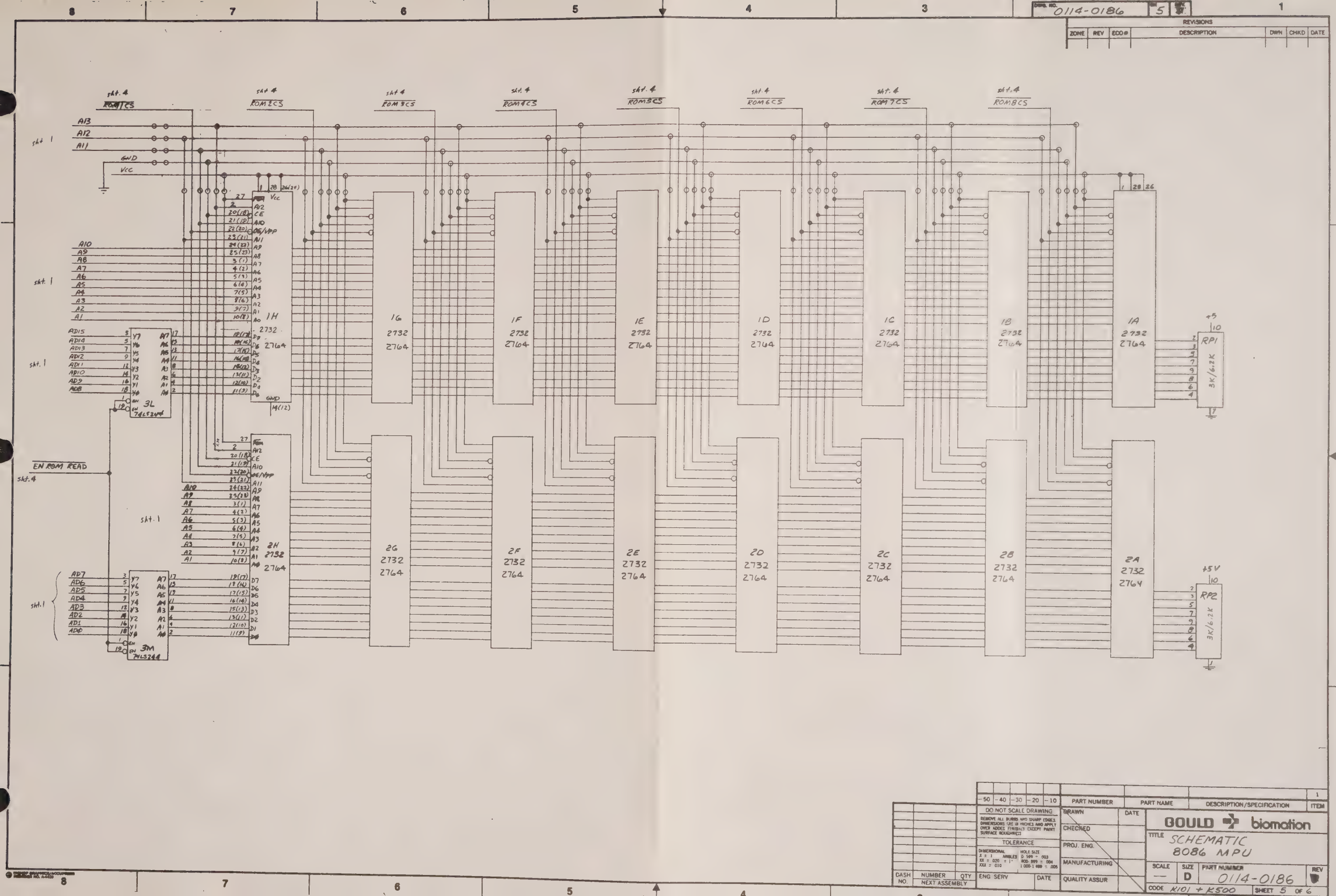
CODE K101 + K500 SHEET 2 OF 6



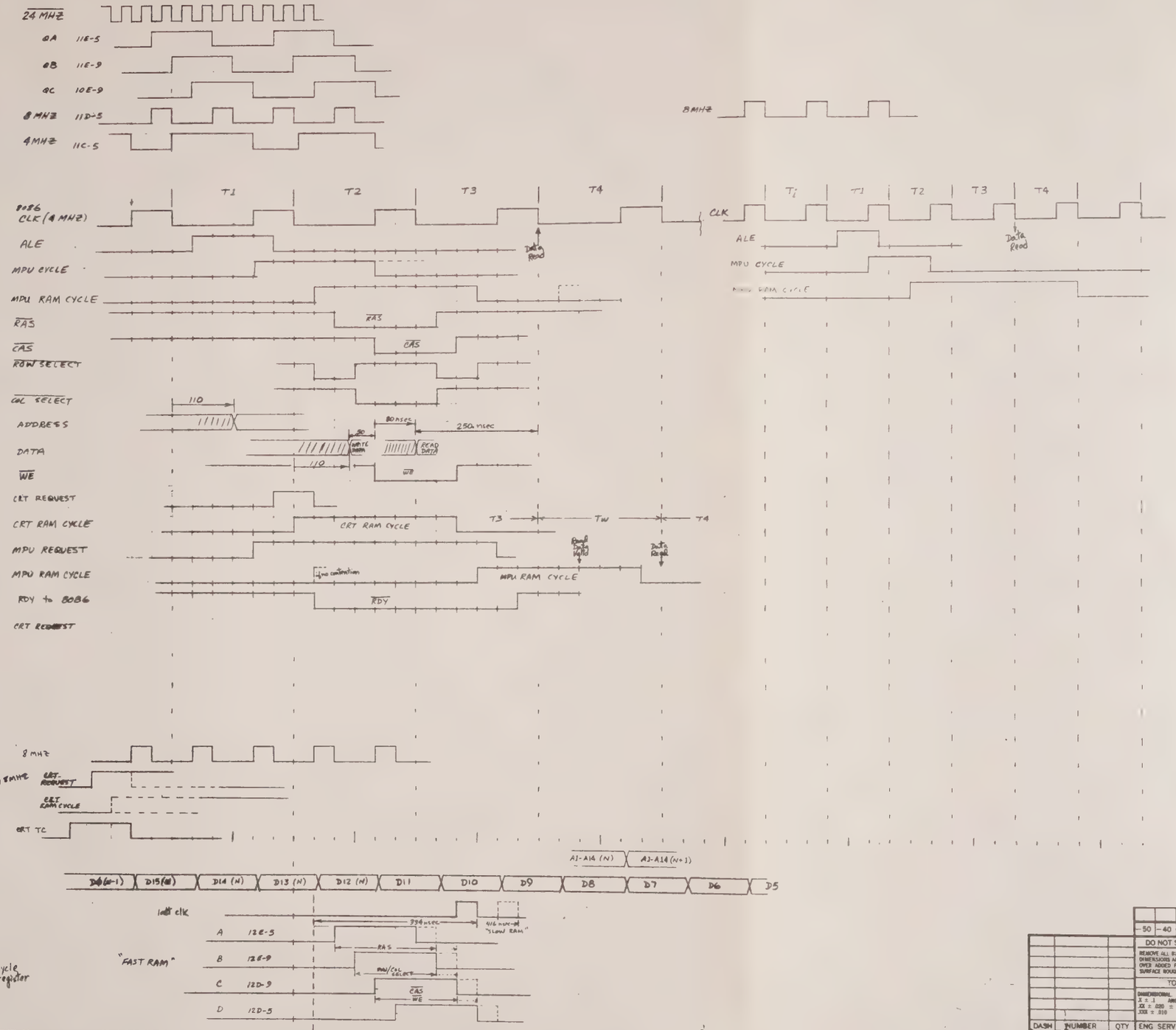
DWG. NO. 0114-0186
SH 3
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
CRT COL SELECT
CRT ROW SELECT
MPU COL SELECT
MPU ROW SELECT
CRT LATCH ENABLE
MPU LATCH ENABLE
to sht. 2
CRT TC
CRT RAM REQUEST
CRT RAM CYCLE
RAM CYCLE
MPU RAM CYCLE
CRT CYCLE
MPU CYCLE
CAS Φ
CAS 1
WE 1 H
WE 1 L
WE Φ H
WE Φ L
RAM WRITE DATA EN
RAS
RAM PAGE 1
DT/R
fm sht. 1
fm sht. 4
SHT 1 ALE
SHT 4 RAM ADRS
NMI to 8086 to SHT 1
MPU RESET SHT 1
RESET SWITCH
BRESET
GND3
P14-79 PUP
P14-80
P14-15
P14-16
P14-75
P14-78
8 MHZ to CRT P14-74
8MHZ CLK to sht 2,4
READY to 8088 to sht 1
SLOW RAM
FAST RAM
last clock
IN = FAST RAM
OUT = SLOW RAM
TO 8086 SLIGHTLY DELAYED, MORE DELAYED ON ↓ EDGE.
BALE P14-84
UNUSED
24 MHZ IN
24 MHZ OUT
Y1 24.MHZ
Q1 2N3906
TIMING AND RAM CONTROL
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV.
DASH NO.
NUMBER
NEXT ASSEMBLY
QTY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC - 8086 MPU
SCALE
SIZE D
PART NUMBER 0114-0186
REV V
CODE K101 + K500
SHEET 3 OF 6



DWG. NO. 0114-0186
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
RP6 2.2K
ROM8CS
ROM7CS
ROM6CS
ROM5CS
to sht. 5
from sht. 1
3J
256x4 PROM
82S129
RP14 2.2K
ROM4CS
ROM3CS
ROM2CS
ROM1CS
3K
ALE
SHT 1
RP10 2.2K
RAM PAGE 1
RAM ADRS
to sht. 3
I/O ADRS
IO PAGE
P14-11
EN OFFBOARD DATA
to sht. 1
RAM ADRS
ROM ADRS
S.A.
EN RAM READ
sht. 2
EN ROM READ
sht. 5
EN S.A. READ
sht. 1
10F
512x4 PROM
82S131
74LS04
LS244
TP1-1
-2
-3
-4
-5
-6
-7
TP1-8
S.A.
GND
RD
A15
RESET SW.
to sht. 3
N.C.
fm 8086 sht. 1
RD
WR
DEN
DT/R
M/IO
BRD
GND1
BWR
GND2
BDEN
BDT/R
BM/IO
P14-7
P14-8
P14-9
P14-10
P14-13
P14-14
P14-12
SH. 1
RP9 3K/6.2K
RP7 3K/6.2K
fm sht 1
HLDA
CRT page select (to sht. 2)
to sht. 2
7D
7C
8C
8D
74LS161
CEP CET MR
RP5 2.2K
RP5 2.2K5
RP6 2.2K
R19 220
R20 330
+5V
R21 220
R22 330
DATA DISPLAY INTERFACE
P14-70
PRESET
P14-71
ENABLE
P14-69
1/2 MHZ CLOCK
CRT TC
LOAD
to 74LS166
to sht. 2
7B
8MHZ CLK
fm sht 3
R5 2.2K
R18 2.2K
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL
HOLE SIZE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
DATE
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC - 8086 MPU
SCALE
SIZE D
PART NUMBER 0114-0186
REV
CODE K101 - K500
SHEET 4 OF 6



DWG. NO. 0114-0186
SH 5
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
sht. 4 ROM1CS
sht. 4 ROM2CS
sht. 4 ROM3CS
sht. 4 ROM4CS
sht. 4 ROM5CS
sht. 4 ROM6CS
sht. 4 ROM7CS
sht. 4 ROM8CS
A13
A12
A11
GND
Vcc
sht. 1
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
3L
74LS244
EN ROM READ
sht. 4
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
3M
74LS244
1H
2732
2764
2H
2732
2764
1G
2732
2764
1F
2732
2764
1E
2732
2764
1D
2732
2764
1C
2732
2764
1B
2732
2764
1A
2732
2764
2G
2732
2764
2F
2732
2764
2E
2732
2764
2D
2732
2764
2C
2732
2764
2B
2732
2764
2A
2732
2764
+5
RP1
3K/6.2K
+5V
RP2
3K/6.2K
DO NOT SCALE DRAWING
TOLERANCE
DASH NO.
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC 8086 MPU
SCALE
SIZE D
PART NUMBER 0114-0186
REV
CODE K101 + K500
SHEET 5 OF 6



TIMING DIAGRAMS

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL	HOLE SIZE
.X ± .1 ANGLES	0.500 ± .003
.XX ± .020 ± 1°	.600-.800 ± .004
.XXX ± .010	1.000-1.400 ± .005

DRAWN | DATE
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV | DATE

DASH NO. | NUMBER | QTY | NEXT ASSEMBLY

GOULD biomation

TITLE SCHEMATIC - 8086 MPU

SCALE — | SIZE D | PART NUMBER 0114-0186 | REV

CODE K101 + K500 | SHEET 6 OF 6

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PRODUCT REL PER ERN # 295	JC	[illegible]	
	B		PRODUCTION RELEASE PER ERN 30[illegible]	[illegible]		
	C	3684A	REV'D PER ECO	MW	DGW	[illegible]
	D	3865	REVISED PER ECO	MW	DGW	8/1/[illegible]
	E	3906	REVISED PER ECO	MW	DGW	8/1/[illegible]
	F	4147	REVISED PER ECO	MW	[illegible]	[illegible]
	G	4425	REVISED PER ECO	JG	[illegible]	[illegible]
	H	4562	REVISED PER ECO Nº	JWC	DGW JMS	6-14-82
	J	4639	PER ECO 7-23-84	George	DGW JMS	[illegible]

JUMPER	AS ETCHED	-20 K101 K102	-30 K105	-40 K205	-10 K500	DESCRIPTION
E1 TO E2	OUT				JUMPER FOR 50HZ ONLY	CRT SCAN RATE IN = 50 HZ. OUT = 60HZ
E3 TO E4	OUT					NOT USED
E5 TO E6	OUT					NOT USED
E7 TO E8	OUT				JUMPER	IN = K500 HORIZ. SCAN OUT = K101
E9 TO E10	OUT					A18
E11 TO E12	IN					A17
E13 TO E14	IN					A16
E15 TO E16	IN					A15 } K101 CMOS RAM
E17 TO E18	IN					A14 } ADDRESS SELECTION
E19 TO E20	IN					A13
E21 TO E22	IN					A12
E23 TO E24	IN					A19
E25 TO E26	IN					A8 } K500 MEM MAPPED I/O
E27 TO E28	IN					A7 } ADDRESS DECODE
E29 TO E30	IN				CUT	IN SELECTS I/O MAPPED I/O (K101)
E30 TO E31	OUT				JUMPER	IN SELECTS MEM MAPPED I/O (K500)
E32 TO E33	IN				CUT	IN FOR K101
E33 TO E34	OUT				JUMPER	IN FOR K500

DASH NO	NUMBER	QTY
-40	0120-0004	1
-30	0117-0003	
-20	0114-0002	
-20	0114-0002	1
-10	0950-0002	1

NEXT ASSEMBLY

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± 1°; XXX = .010

HOLE SIZE: 0 .599 ± .003; 600 .999 ± .004; 1.000-1.499 ± .005

ENG SERV. | DATE

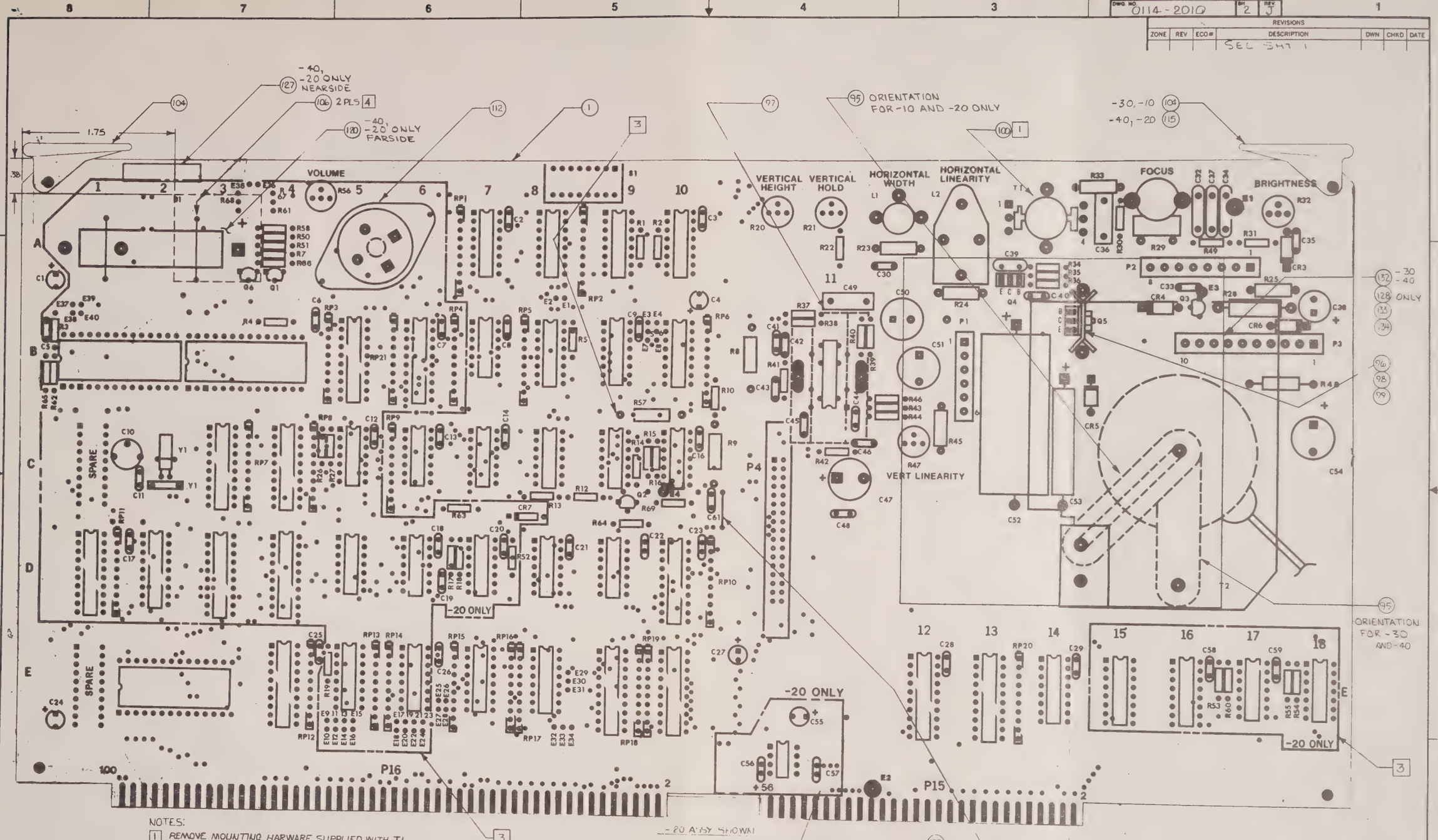
		DATE
DRAWN	DGW	3/26/82
CHECKED	[illegible]	12/6/82
PROJ. ENG.	[illegible]	1/26/83
MANUFACTURING	[illegible]	1/27/83
QUALITY ASSUR	[illegible]	1/27/83

GOULD biomation

TITLE: ASSEMBLY DATA DISPLAY BD

SCALE	SIZE	PART NUMBER	REV
2/1	D	0114-2010	J

CODE K101 / K500 | SHEET 1 OF 2



NOTES:

1. REMOVE MOUNTING HARWARE SUPPLIED WITH T1, USE ITEM 100 TO SECURE TO BOARD
2. IC'S 7E, 9E, RP2 & S1 ARE -10; IC 9E & RP2 ARE -30.
3. COMPONENTS IN THIS AREA PLUS R57 ARE -20, -40 ONLY EXCEPT FOR R26 & R27.
4. SECURE BATTERY, B1, TO BOARD WITH ITEM 106 2 PLACES BEFORE SOLDERING LEADS TO PREVENT STRAIN ON BATTERY LEADS.
5. JUMPER FROM E1 TO E2 AND E3 TO E4 ON SOLDER SIDE OF BOARD [illegible] AS SHORT AS POSSIBLE.

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°; HOLE SIZE: 0.599 - .003, 600.999 - .004, 1.000 1.499 - .005

DRAWN: J W CARROLL — DATE: 12-6-82

CHECKED: [illegible] — 12/1/82

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

ENG SERV. — DATE

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

GOULD — Instruments Division, Santa Clara Operations

TITLE: ASSEMBLY DATA DISPLAY BOARD

SCALE: 2/1 | SIZE: D | PART NUMBER: 0114-2010 | REV: J

MODEL

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER D75AR

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER D75AR

K205 K105, K101, K500

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1			1	1	1	1	0114-2012	PWB				
2			3	2	3	2	3000-2000	RESISTOR	R35, 36 [1] R64		200Ω, ¼W, 5%	
3			1	1	1	1	3000-3307	RESISTOR	R38		3.3Ω, 1/4W, 5%	
4			2	2	2	2	3050-4700		R8, 9		470Ω, ½W, 5%	
5			1	1	1	1	3000-8206		R12		82Ω, ¼W, 5%	
6			2	2	2	2	-4700		R5, 34		470Ω	
7			12	2	12	2	-2201		[2] R1, 2 [1] R19, 1, 2, 53-55, 58, 3, 4, 60, 62, 65		2.2K	
8			4	—	4	—	-1002		R17, 18, 52, 63		10K	
9			1	1	1	1	-5601		R46		5.6K	
10			2	2	2	2	-8201		R39, 40		8.2K	
11			2	2	2	2	-4702		R43, 44		47K	
12			1	1	1	1	-1203		R22		120K	
13			2	2	2	2	-2203		R37, 41		220K	
14			1	1	1	—	-2703		R42		270K	
15			1	1	1	1	-5103		R31		510K	
16			—	—	—	1	-6803		R42		680K	
17			2	2	2	2	3000-1004	RESISTOR	R30, 49		1MEGΩ, ¼W, 5%	
18			1	1	1	1	3050-2200	RESISTOR	R24		220Ω, ½W, 5%	

COMMENTS	TOTAL COST	UNIT COST
[1] USED ON -20 AND -40		
[2] USED ON -10 ONLY		
-10 K500		
-20 K101/K102		
-30 K105		
-40 K205		
[3] -10 - 30		

ASSEMBLY TIME	COMPONENT LEAD SPACING
	¼W RES -.40 ⅛W RES -.40 ½W RES -.50 1W RES -.70

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROD. REL PER ERN # 295	12/6/2	M.W.	12/8R	
B	" " " " # 302				
C	REVISED PER ECO # 3684A	5/2/83	MW	DGW	5/4/83
D	REVISED PER ECO # 3865	7/28/3	MW	DGW	8/1/83
E	REVISED PER ECO # 3906	11/29/3	MW	DGW	11/1/83
F	REVISED PER ECO # 4147	11/22/83	MW	DGW	12/1/83
G	REVISED PER ECO # 4425	3-14-84	J.G.	TK	JMS 3/20/84

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	
-40	0120-0004	1
-20	0114-1002	1
-30	0117-0003	1
-20	0114-0002	1
-10	0950-0002	1

	DATE
DRAWN M.W	11/82
CHECKED C. Hewson	11/4/82
ENGINEER Curt	11/26/83
MANUFACTURING	12/1/83
QUALITY ASSURANCE	11/27/83

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 1 OF 8

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER D75AR

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER D75AR

ITEM	QUANTITY PER ASSEMBLY 60	-50	-40	30	20	10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYP
19			1	1	1	1	3050-1007	RESISTOR	R45		1.0 Ω, ½W, 5%	
20			2	1	2	1	3050-3906		R25 [1] R57		39Ω, ½W, 5%	
21			1	1	1	1	3050-1000		R33		100Ω, ½W, 5%	
22			1	1	1	1	SELECTED AT TEST		R23		S.A.T.	
23			2	—	2	—	3000-2202		R67, 68		22K, ¼W, 5%	
24			1	1	1	1	3200-0008		R48		1.0 Ω, 1W, 3%	
25			1	1	1	1	3070-1501		R28		1.5 KΩ, 1W, 5%	
26			1	1	1	1	3100-7500		R13		.75 Ω, ⅛W, 1%	
27			1	1	1	1	3100-6040		R14		604	
28			1	1	1	1	3100-8250		R15		825	
29			1	1	1	1	3100-9090	RESISTOR	R16		909Ω, ⅛W, 1%	
30			1	1	1	1	3300-0084	RES. VAR.	R47		50K	
31			3	3	3	3	3300-0085		R20, 21, 32		100K	
32			1	1	1	1	3300-0088	RES. VAR.	R29		1MEG	
33			1	1	1	1	4100-0024	CAPACITOR	C43		68 PF, 500V MKA	
34			1	1	1	1	4100-0002		C39		470PF, 500V MICA	
35			8	6	8	6	4000-0009		C33, 35, 42, 44-46 [1] C5, 6		0.1MF, 100V	
36			5	4	5	4	4400-0043	CAPACITOR	C1, C4, C24, C27 [1] C19		47 UF, 6V	

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APP
H	REV'D PER ECO NO 4562	6-28-84	JMS	DGW	JMS
J	PER ECO 4639	7-23-84	MOLFE	DGW	JMS

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN M. WOLFE	11/22/82
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 2 OF 8

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 075AP

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 075AP

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37			2	2	2	2	4000-0042	CAPACITOR	C36,49		.15µF, 100V	
38			—	—	—	1	4400-0039		C50		10uf / 16V	
39			3	3	3	3	4000-0043		C32,34,37		.01µF, 500V	
40			26	17	26	17	4010-0103		C40,41,2,3,8,9,13,4,6,21-23,25,26,28,29,48 [1] C7,12,17,18,20,56,57,58,59		.01µF, 50v	
41			1	—	1	—	4010-0100		C11		10pf, 100v	
42			1	1	1	1	4400-0036		C51		1000µF, 16V	
43			2	2	2	2	4400-0037		C47,54		470µF, 25V	
44			1	1	1	—	4400-0047		C50		220µF, 35v	
45			1	1	1	1	4200-0036-10	CAPACITOR	C52		6µF, 200V	
46			1	1	1	1	4400-0038	CAPACITOR	C38		10uf, 100V	
47			1	—	1	—	7000-0451	BATTERY	B1	POWER CONV INC.	2.4V NICD	
48			1	1	1	1	1200-0033	DIODE	CR5	3BF4		
49			3	3	3	3	1200-0031	DIODE	CR3,4,6	IN4937		
50			1	1	1	1	4300-0041	CAPACITOR	C53		.056µf, 400V	
51			1	—	1	—	3000-3900	RESISTOR	R66		390Ω, ¼W, 5%	
52			3	1	3	1	6100-0151	SOCKET	X2E/[1] X1B, X3B		28 PIN	
53			1	1	1	1	SELECTED AT TEST	CAPACITOR	C30		S.A.T.	
54			1	—	1	—	4600-0010	CAP, VAR	C10		7-40 pf	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M. WOLFE 11/22/82
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 3 OF 8

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 075AH

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 075AH

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	40	30	20	10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55			2	1	2	1	1300-0028	TRANSISTOR	Q2, [1] Q6	2N3904		
56			1	—	1	—	1400-0019		Q1	2N3906		
57			1	1	1	1	1300-0049		Q5	BV407		
58			1	1	1	1	1300-0048	TRANSISTOR	Q4	2N4921		
59			2	2	2	3	6100-0120	SOCKET	X9 [2] [1] X8B, X10B		16 PIN	
60			1	—	1	—	3000-6800	RESISTOR	R51		680Ω, ¼W, 5%	
61			—	—	—	1	0950-0195	IC	10B		PROM, HORIZ	
62			8	8	8	8	3700-0083	RESISTOR PACK	RP1,5,6,8,12,15,20, [2] RP2 [1] RP14		2.2KΩ, 10 PIN SIP	
63			5	—	5	—	3700-0085		RP3,7,8,11,21		22KΩ 10 PIN SIP	
64			7	5	7	5	3700-0049	RESISTOR PACK	RP10,16-19 [1] RP4,13		3K/6.2KΩ 10PIN SIP	
65			1	1	1	1	1500-0018	TRANSISTOR	Q3		VN10KM	
66			1	1	1	1	1800-0105	I.C.	7C	74LS00		
67			1	1	1	1	1800-0123		6C	74LS14		
68			2	1	2	1	-0110		9D [1] 5D	74LS10		
69			1	1	1	1	-0111		8D	74LS20		
70			2	1	2	1	-0115		7B [1] 17E	74LS74		
71			2	—	2	1	-0254		[2] 7E [1] 5E, 16E	74LS85		
72			1	1	1	1	1800-0404	I. C.	9C	74LS136		

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M. WOLFE 11/22/82
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 4 OF 8

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 075AR

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 075AR

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
73			1	1	1	1	1800-0301	I.C.	14E	74LS156		
74			6	4	6	4	-0125		7A-10A [1] 15E,16E	74LS161		
75			1	1	1	1	-0121		9B	74LS175		
76			3	2	3	2	-0267		10D, 4E - [1] 6B	74LS240		
77			3	2	3	2	-0240		13E, [4] 9E [1] 5B, [1] 1D	74LS244		
78			3	1	3	1	-0268		10E [1] 3C, 4C	74LS245		
79			3	—	3	1	-0231		12E [1] 3D 4D	74LS273		
80			1	1	1	1	-0193		8E	74LS138		
81			2	1	2	1	-0097		10C [1] 18E	7406		
82			1	1	1	1	1800-0038		8C	74S20		
83			1	—	1	—	0114-0064		8B		PROM, VERTICAL	
84			2	—	2	—	1820-0080		18,3B		IC/ST RAM CMOS	
85			1	1	1	1	1800-0319		2E	8259-A		
86			1	—	1	—	0114-0065		10B		PROM, HORIZONTAL	
87			1	1	1	1	1700-0082		11B	TDA-1270	VERTICAL PROCESSOR	
88			1	—	1	—	1800-0341		2D	MSM5832		
89			1	—	1	—	1800-0311	I.C.	7D	7438		
90			—	—	—	1	0950-0194	I.C.	8B		PROM, VERT	

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DRAWN M. WOLFE 11/22/82
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 5 OF 8

DRAWING NUMBER

DRAWING NUMBER

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	20	10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
91			1	1	1	1	9000-0049	COIL ASSY, WTH	L1		5-30 uH	
92			1	1	1	1	0113-0011	COIL ASSY, LIN	L2			
93			1	—	1	—	5100-0018	CRYSTAL	Y1		32.768 KHz	
94			1	1	1	1	0113-0014	TRANSFORMER	T1			
95			1	1	1	1	9000-0082	TRANSFORMER	T2		FLYBACK	
96			1	1	1	1	7000-0365	HEATSINK	@Q5			
97			1	1	1	1	7000-0366	HEATSINK	@11B			
98			1	1	1	1	7000-0221	INS. WASH	@Q5			
99			1	1	1	1	7200-0017	INSULATOR	@Q5			
100			1	1	1	1	2400-0004	MTG BRACKET	@T1			
101			1	1	1	1	6000-0359-6	HEADER	P1		6PIN	
102			1	1	1	1	6000-0359-8		P2		8PIN	
103			1	1	1	1	6000-0359-10	HEADER	P3		10PIN	
104			1	2	1	2	7000-0120	EJECTOR				
105			1	1	1	1	9000-0094	GND WIRE				
106			2	—	2	—	7200-0032	MOUSE TAIL			.115 DIA, 4"	
107			—	—	—	1	6600-0037	DIP SWITCH	S1			
108			2	2	2	2	3000-1001	RESISTOR	R10,69		1K, 1/4W, 5%	

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DRAWN M. WOLFE 11/22/82
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 6 OF 8

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER D75AR

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER D75AR

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
109			1	1	1	1	3000-2200	RESISTOR	R26		220Ω, 1/4W, 5%	
110			1	1	1	1	3000-3300	RESISTOR	R27		330Ω, 1/4W, 5%	
111			1	—	1	—	3300-0096	RES., VAR.	R56		1K, 1 TURN	
112			1	—	1	—	7400-0002	BEEPER				
113			1	—	1	—	1700-0071	I.C.	11C		LF356	
114			1	—	1	—	4400-0045	CAPACITOR	C55		33μf, 25v	
115			1	—	1	—	0112-0228-08	EJECTOR, STAMPED			"A8"	
116			1	—	1	—	1800-0351	I.C.	5C		74LS12	
117			1	—	1	—	1800-0352	I.C.	6D		74LS22	
118			1	—	1	—	3000-5106	RESISTOR	R61		51Ω, 1/4W. 5%	X
119			1	—	1	—	1000-0002	DIODE	CR7		IN4152	X
120			0.1	—	0.1	—	8300-0027	INSULATION	3M4108		1"x 1" x 1/8" THK	
121			1	—	1	—	4000-0011	CAPACITOR	C61		2.2 μf	
122			1	—	1	—	6000-0389	HEADER	P4		34 PIN - FLOPPY	
123			1	—	1	—	6100-0146	SOCKET	2D		18 PIN	
124												
125			1	—	1	—	3000-2700	RESISTOR	R7		270Ω, 1/4W, 5%	
126			1	—	1	—	3000-3301	RESISTOR	R50		3.3K 1/4W. 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	M. WOLFE	11/22/82	
CHECKED			
ENGINEER			
MANUFACTURING			
QUALITY ASSURANCE			

DASH NO. | NUMBER NEXT ASSEMBLY | QTY

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 7 OF 8

DRAWING NUMBER

DRAWING NUMBER

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
127						·	—	1	—	0114-0432	LABEL, CAUTION NICD ONLY!		1
128						2	2	—	—	7011-1440-10	SCREW 4-40X5/16 PH		X
129						1	1	—	—	0117-0149-10	PROM, VERT, K105	8B	
130						1	1	—	—	0117-0150-10	PROM, HORIZ, K105	10B	
131													
132						1	1	—	—	0117-0139-10	SHIELD, DEFLECTION		X
133						2	2	-	-	7084-1004-00	#4 STAR WASHER		X
134						2	2	-	-	7080-1004-00	#4 SMALL WASHER		X
135						—	—	REF	—	30 AWG KYNAR	JUMPER WIRE	PIN 19 2D (REF SHT 6 SCHEM.)	
136						1.3	1.3	1.3	1.3	7150-0018-09	WIRE 19 STRAND WHITE	SEE NOTE 5	

NOTES

LIST OF MATERIAL
DATA DISPLAY PWA ASSY

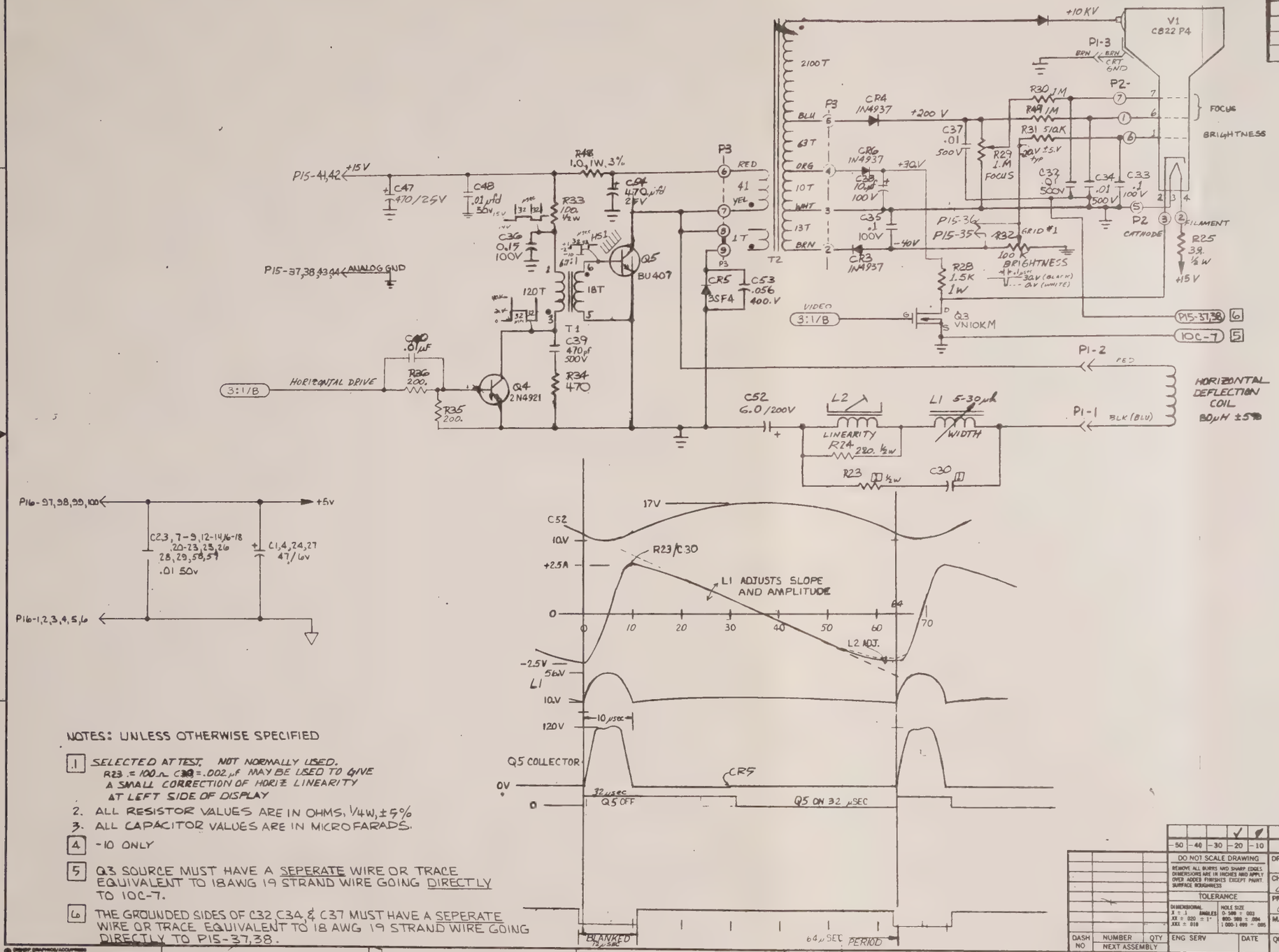
GOULD → biomation

B | 0114-2010 | REV J

MODEL K101/K500 | SHEET 8 OF 8

KLINGLER VR M10

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PRODUCTION RELEASE, ERN#295	[illegible]	[illegible]	
	B		PRODUCTION RELEASE ERN#302	[illegible]		
	C	3684A	REV'D PER ECO	MW	DLW	5/4/83
	D	3865	REVISED PER ECO	MW	DLW	8/1/83
	E	3906	REVISED PER ECO	MW	DLW	8/1/83
	F	4147	REVISED PER ECO	MW	[illegible]	11/13/83
	G	4425	REVISED PER ECO	J.G.	[illegible]	[illegible]
	H	4562	REVISED PER ECO NO	JWC	[illegible]	6-18-84
	J	4639	PER ECO	[illegible]	[illegible]	7/24/84



NOTES: UNLESS OTHERWISE SPECIFIED

1. SELECTED AT TEST. NOT NORMALLY USED. R23 = 100Ω C30 = .002µf MAY BE USED TO GIVE A SMALL CORRECTION OF HORIZ LINEARITY AT LEFT SIDE OF DISPLAY
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. -10 ONLY
5. Q3 SOURCE MUST HAVE A SEPERATE WIRE OR TRACE EQUIVALENT TO 18AWG 19 STRAND WIRE GOING DIRECTLY TO 10C-7.
6. THE GROUNDED SIDES OF C32, C34, & C37 MUST HAVE A SEPERATE WIRE OR TRACE EQUIVALENT TO 18 AWG 19 STRAND WIRE GOING DIRECTLY TO P15-37,38.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			✓	✓				1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL .X ± .1 .XX ± .020 .XXX ± .010 ANGLES ± 1° HOLE SIZE 0-.500 ± .003 .500-.999 ± .004 1.000-1.499 ± .005

DASH NO	NUMBER	QTY	ENG SERV	DATE
	NEXT ASSEMBLY			

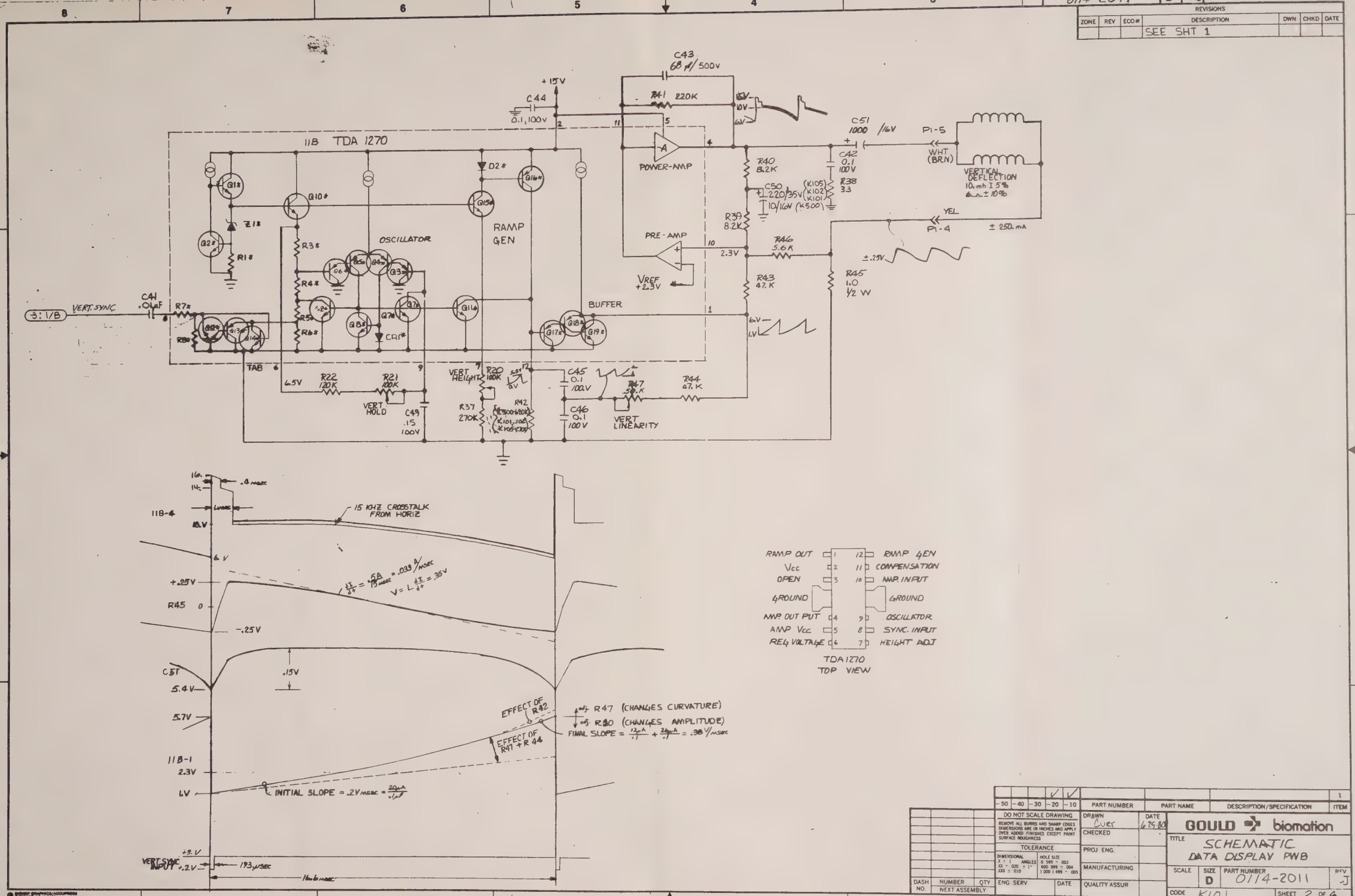
		DATE
DRAWN	CURT	6-25-80
CHECKED	[illegible]	12/9/82
PROJ. ENG	Curt	1/26/83
MANUFACTURING		
QUALITY ASSUR	[illegible]	1/27/83

GOULD biomation

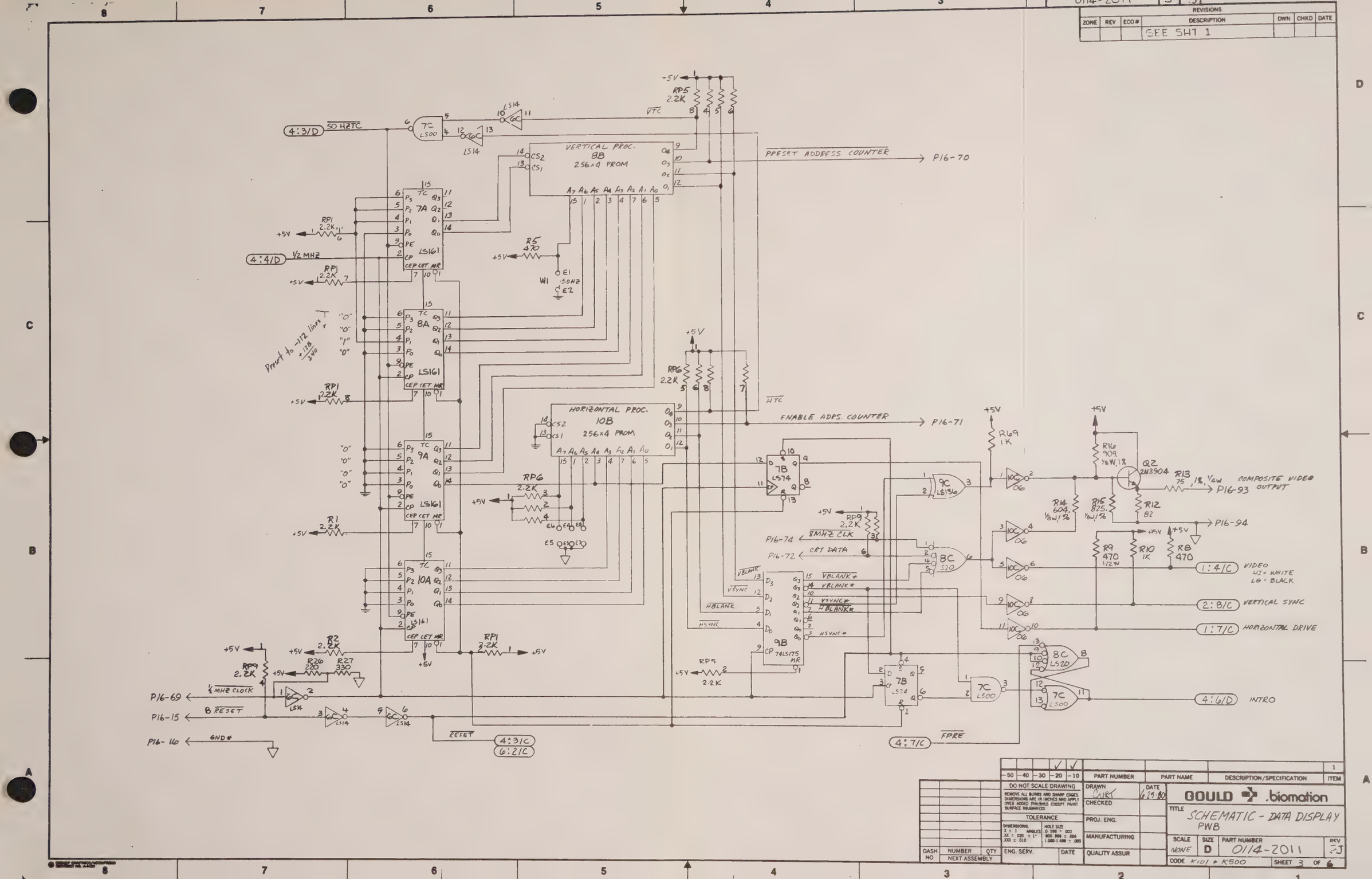
TITLE SCHEMATIC DATA DISPLAY PWB

SCALE	SIZE	PART NUMBER	REV
	D	0114-2011	J

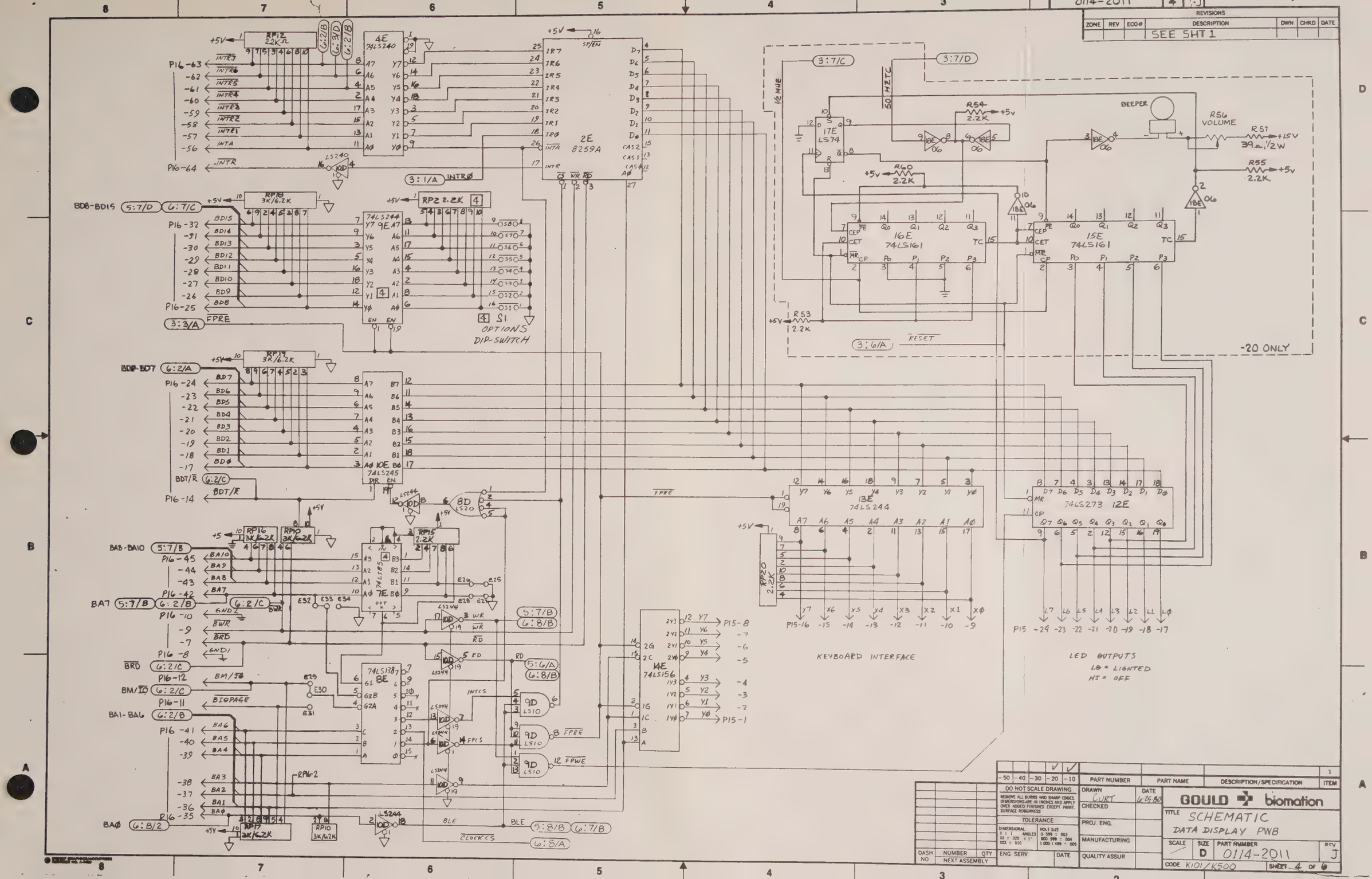
CODE K101 + K500 SHEET 1 OF 5



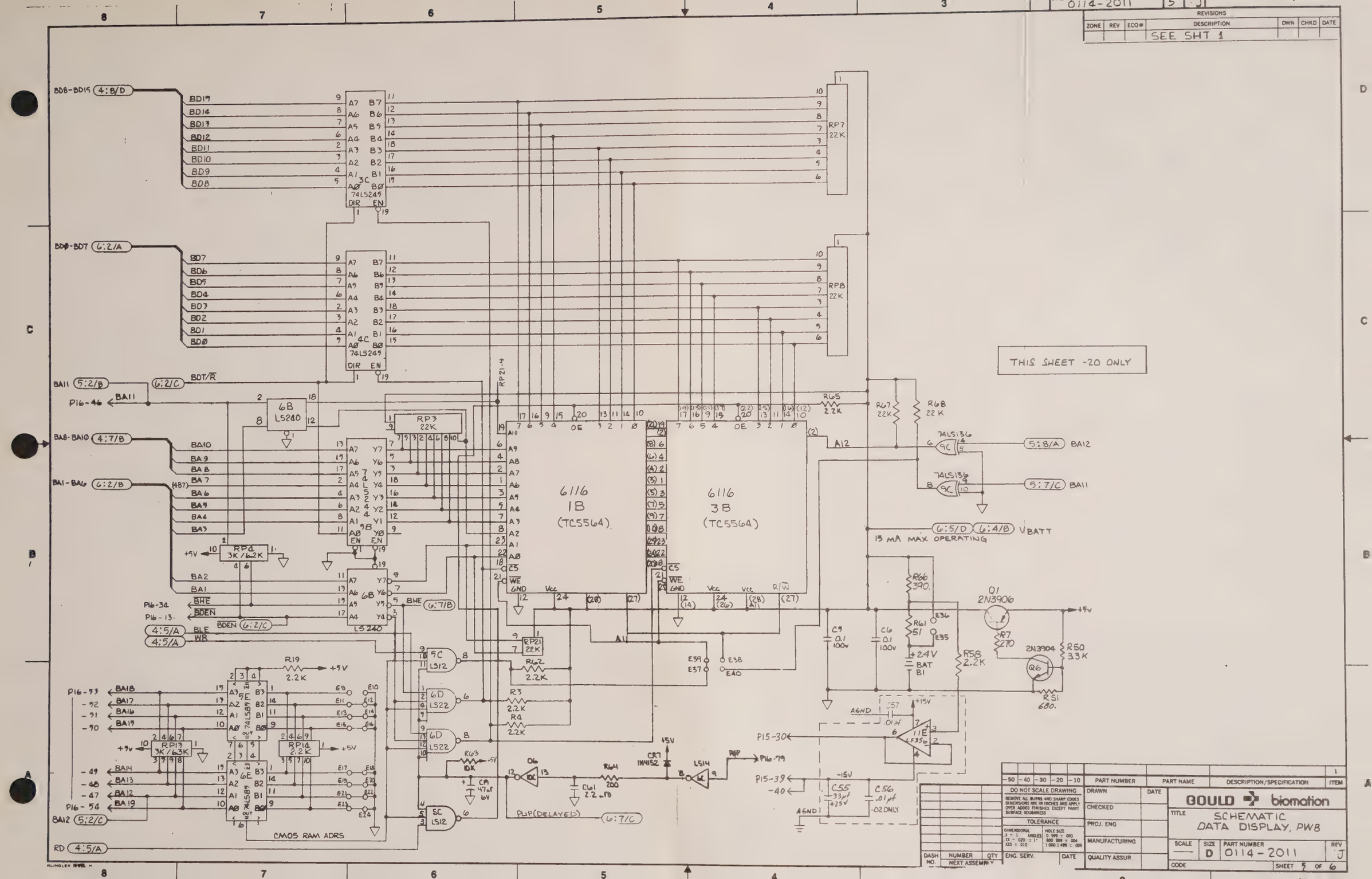
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
11B TDA 1270
C43 68 µf/500V
+15V
C44 0.1, 100V
R41 220K
POWER-AMP
PRE-AMP
VREF +2.3V
C51 1000 /16V
P1-5
WHT (BRN)
VERTICAL DEFLECTION 10 mh I 5% 6Ω ± 10%
C42 0.1 100V
R38 33
R40 8.2K
C50 220/35V (K105) (K102) (K101) 10/16V (K500)
R39 8.2K
YEL
P1-4
± 250 mA
R46 5.6K
±.25V
R43 47.K
R45 1.0 1/2 W
BUFFER
OSCILLATOR
RAMP GEN
D2*
Q1*
Q10*
Q15*
Q16*
Z1*
Q2*
R1*
R3*
R4*
R5*
R6*
Q6*
Q4*
Q3*
Q8*
Q7*
Q11*
Q17*
Q18*
Q19*
CR1*
3:1/B
VERT. SYNC
C41 .01µF
R7*
R8*
TAB
6.5V
R22 120K
R21 100K
VERT HOLD
C49 .15 100V
VERT HEIGHT
R20 100K
R37 270K
R42
C45 0.1 100V
C46 0.1 100V
R47 50.K
VERT LINEARITY
R44 47.K
6.V
1.V
11B-4
15 KHZ CROSSTALK FROM HORIZ
.4 msec
6 V
+.25V
R45 0
-.25V
C51
5.4V
5.7V
.15V
11B-1
2.3V
1.V
EFFECT OF R42
EFFECT OF R47 + R44
adj. R47 (CHANGES CURVATURE)
adj. R50 (CHANGES AMPLITUDE)
FINAL SLOPE = 12µA/.1 + 26µA/.1 = .38 V/msec
INITIAL SLOPE = .2V msec = 20µA/.1µf
VERT SYNC INPUT
+3.V
+.2V
193 µsec
16.6 msec
RAMP OUT
Vcc
OPEN
GROUND
AMP. OUT PUT
AMP Vcc
REG VOLTAGE
RAMP GEN
COMPENSATION
AMP. INPUT
GROUND
OSCILLATOR
SYNC. INPUT
HEIGHT ADJ
TDA 1270 TOP VIEW
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL X ± .1 ANGLES XX ± .020 ± 1° XXX ± .010
HOLE SIZE 0.599 ± .003 600.999 ± .004 1.000 1.499 ± .005
DRAWN CURT DATE 6-25-80
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV DATE
DASH NO. NUMBER QTY NEXT ASSEMBLY
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
GOULD biomation
TITLE SCHEMATIC DATA DISPLAY PWB
SCALE SIZE D PART NUMBER 0114-2011 REV J
CODE K101 SHEET 2 OF 6



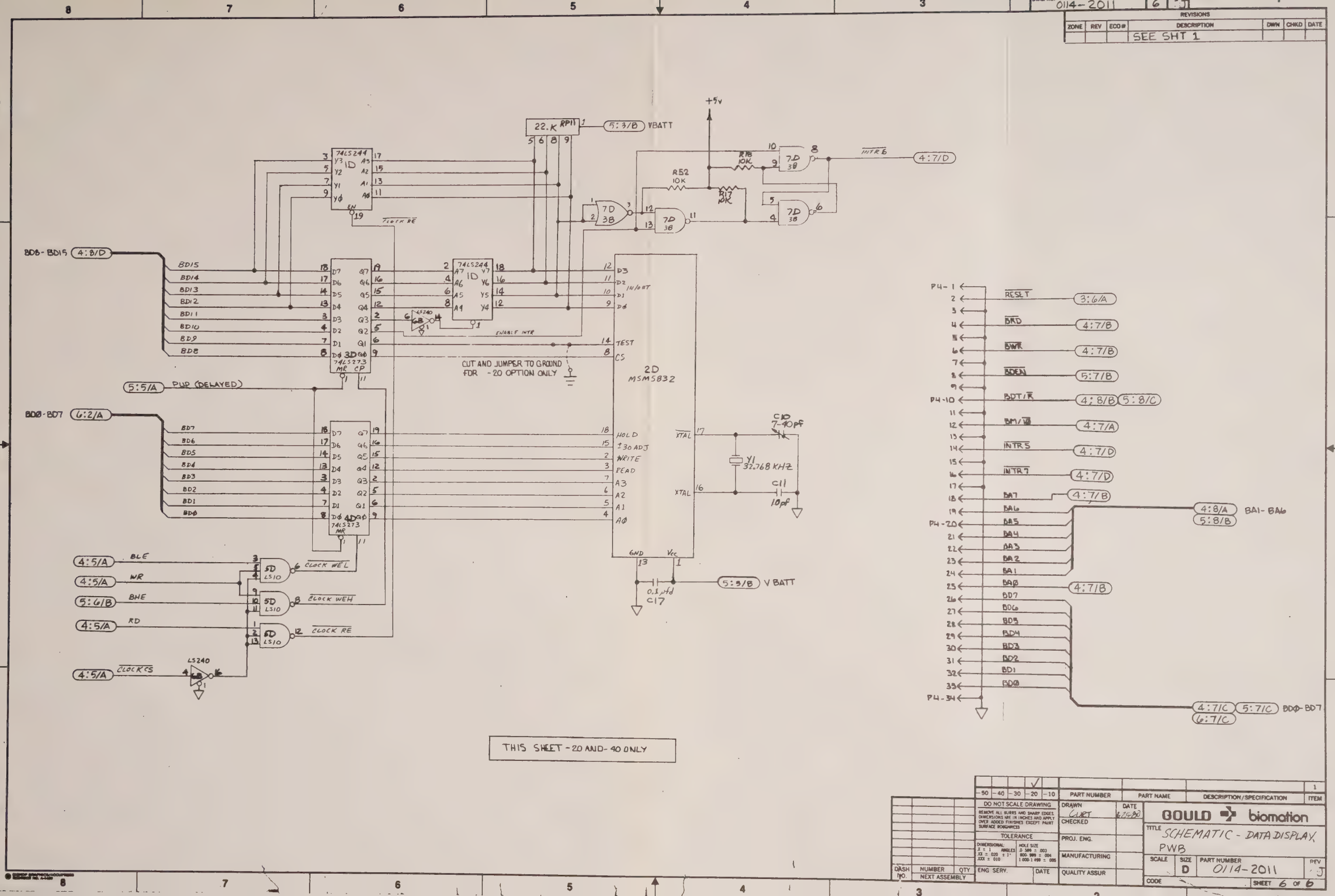
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
VERTICAL PROC. 8B 256x4 PROM
HORIZONTAL PROC. 10B 256x4 PROM
PRESET ADDRESS COUNTER
ENABLE ADRS. COUNTER
P16-70
P16-71
P16-93
P16-94
COMPOSITE VIDEO OUTPUT
VIDEO HI = WHITE LO = BLACK
VERTICAL SYNC
HORIZONTAL DRIVE
INTRO
8MHZ CLK
CRT DATA
P16-74
P16-72
P16-69
P16-15
P16-16
1/2 MHZ CLOCK
B RESET
GND#
RESET
FPRE
4:3/D 50 HZTC
4:4/D 1/2 MHZ
4:3/C
6:2/C
4:7/C
Preset to -112 lines
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV.
DATE
GOULD biomation
TITLE SCHEMATIC - DATA DISPLAY PWB
SCALE NONE
SIZE D
PART NUMBER 0114-2011
REV
CODE K101 + K500
SHEET 3 OF 6



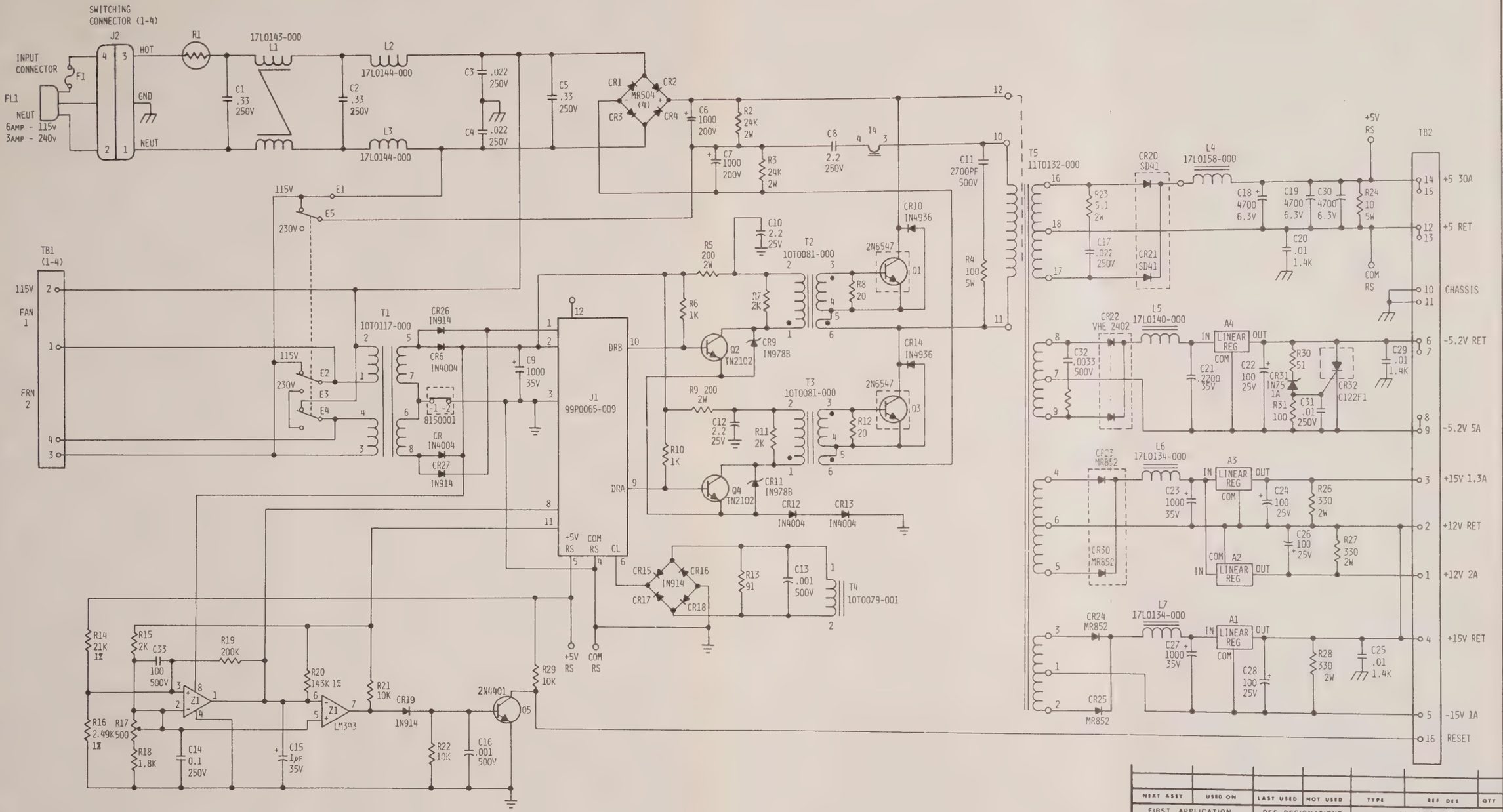
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
2E 8259A
4E 74LS240
RP12 2.2K
RP18 3K/6.2K
RP19 3K/6.2K
RP16 3K/6.2K
RP10 3K/6.2K
RP17 3K/6.2K
RP15 2.2K
RP2 2.2K
RP20 2.2K
RP6-2
S1 OPTIONS DIP-SWITCH
17E LS74
16E 74LS161
15E 74LS161
13E 74LS244
12E 74LS273
14E 74LS156
8E 74LS138
7E 74LS85
8D LS20
9D LS10
BEEPER
R56 VOLUME
R57 39Ω 1/2W
R54 2.2K
R60 2.2K
R53 2.2K
R55 2.2K
-20 ONLY
KEYBOARD INTERFACE
LED OUTPUTS
LO = LIGHTED
HI = OFF
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PRINT. SURFACE ROUGHNESS
TOLERANCE
DRAWN CURT
DATE 6-25-80
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC
DATA DISPLAY PWB
SCALE
SIZE D
PART NUMBER 0114-2011
REV J
CODE K101/K500
SHEET 4 OF 6



0114-2011
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
THIS SHEET -20 ONLY
BD8-BD15 4:8/D
BD0-BD7 6:2/A
BA11 5:2/B
BA8-BA10 4:7/B
BA1-BA6 6:2/B
BDT/R
P16-46
BA11
BA12
BA10
BA9
BA8
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BHE
BDEN
BLE
WR
P16-34
P16-13
4:5/A
4:5/A
BHE 6:7/B
BDEN 6:2/C
3C 74LS245
4C 74LS245
5B 74LS244
6B LS240
RP7 22K
RP8 22K
RP3 22K
RP4 3K/6.2K
RP21 22K
RP13 3K/6.3K
RP14 2.2K
6116 1B (TC5564)
6116 3B (TC5564)
5C LS12
6D LS22
6D LS22
5C LS12
CMOS RAM ADRS
RD 4:5/A
BA12 5:2/C
P16-53
P16-54
BA18
BA17
BA16
BA15
BA14
BA13
BA12
BA19
R19 2.2K
R62 2.2K
R3 2.2K
R4 2.2K
R63 10K
C19 47uF 6V
Q6 10C
C61 2.2uFD
R64 200
CR7 1N4152
LS14
PUP
PUP(DELAYED) 6:7/C
R65 2.2K
R67 22K
R68 22K
74LS136
5:8/A BA12
5:7/C BA11
6:5/D 6:4/B VBATT
15 MA MAX OPERATING
R66 390.
R61 51
2.4V BAT B1
C5 0.1 100v
C6 0.1 100v
R58 2.2K
Q1 2N3906
R7 270
2N3904 Q6
R50 3.3K
R51 680.
C57 .01pf
11E LF356
P15-30
P15-39
-40
C55 33pf +25V
C56 .01pf -02 ONLY
AGND
+15V
-15V
+5V
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL .X ± .1 .XX ± .020 .XXX ± .010
ANGLES ± 1°
HOLE SIZE 0.599 ± .003 .600 .999 ± .004 1.000 1.499 ± .005
ENG. SERV.
DASH NO. NUMBER QTY NEXT ASSEMBLY
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
DRAWN DATE
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC DATA DISPLAY, PW8
SCALE SIZE D PART NUMBER 0114-2011 REV J
CODE
SHEET 5 OF 6



0114-2011
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
22.K RP11
5:3/B VBATT
+5v
74LS244
1D
R18 10K
R52 10K
R17 10K
7D 38
INTR 6
4:7/D
CLOCK RE
BD8-BD15 4:8/D
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
3D 74LS273
MR CP
LS240
ENABLE INTR
CUT AND JUMPER TO GROUND FOR -20 OPTION ONLY
2D MSM5832
D3
D2
D1
D0
IN/OUT
TEST
CS
HOLD
±30 ADJ
WRITE
READ
A3
A2
A1
A0
XTAL
GND
Vcc
C10 7-40pf
Y1 32.768 KHZ
C11 10pf
0.1 μfd C17
5:3/B V BATT
5:5/A PUP (DELAYED)
BD0-BD7 6:2/A
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
4D 74LS273
MR
4:5/A BLE
4:5/A WR
5:6/B BHE
4:5/A RD
4:5/A CLOCK CS
5D LS10
CLOCK WEL
CLOCK WEH
CLOCK RE
LS240
P4-1
RESET 3:6/A
BRD 4:7/B
BWR 4:7/B
BDEN 5:7/B
P4-10
BDT/R 4:8/B 5:8/C
BM/IO 4:7/A
INTR5 4:7/D
INTR7 4:7/D
BA7 4:7/B
BA6
P4-20
BA5
BA4
BA3
BA2
BA1
BA0 4:7/B
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
P4-34
4:8/A 5:8/B BA1-BA6
4:7/C 5:7/C 6:7/C BD0-BD7
THIS SHEET -20 AND -40 ONLY
-50 -40 -30 -20 -10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: .X ± .1 .XX ± .020 .XXX ± .010
ANGLES ± 1°
HOLE SIZE .0 .500 ± .003 .000 .999 ± .004 1.000-1.499 ± .005
DRAWN CURT
DATE 6-25-80
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV.
DATE
DASH NO.
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC - DATA DISPLAY, PWB
SCALE
SIZE D
PART NUMBER 0114-2011
REV J
CODE
SHEET 6 OF 6



REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

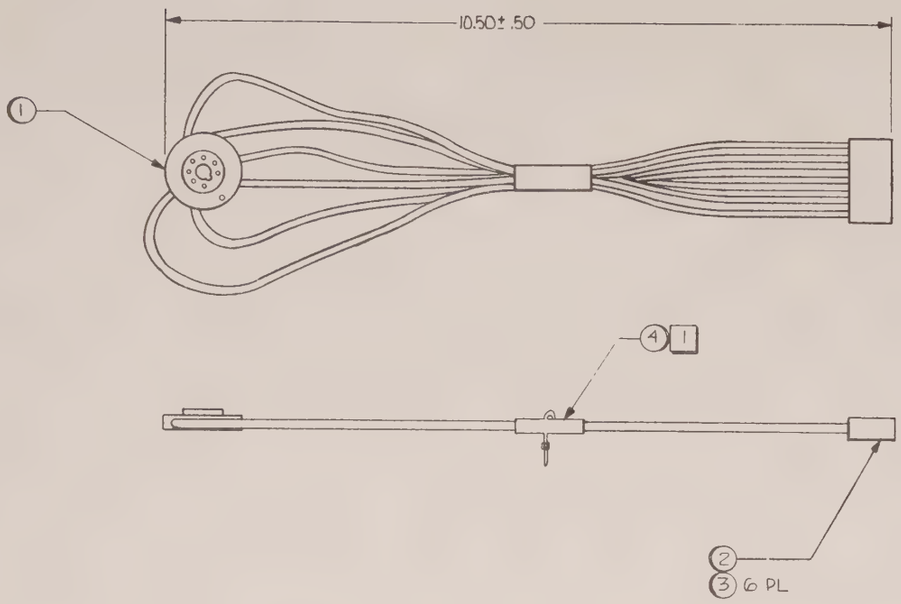
NEXT ASSY	USED ON	LAST USED	NOT USED	TYPE	REF DES	QTY
FIRST APPLICATION		REF DESIGNATIONS		SPARE GATES		

APPROVALS	DATE
DRAWN	10-7-83
CHECKED	
ENGR	

SCHEMATIC K105-D POWER SUPPLY

SIZE D | DWG NO 0117-0377 | REV

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 309	STM	[illegible]	2/2/83
	A	3957	PROD REL PER ECO # [illegible]	STM	[illegible]	9/16/83



WIRING CODE	
PIN	COLOR
1	ORG
2	BRN
3	VIO
4	N/C
5	BLK
6	GRN
7	BLU
8	N/C

1 MARK PART WITH PART NO. 0117-0021 DASH NO. & REV LEVEL USING 1/8" CHARACTERS.

NOTES: UNLESS OTHERWISE SPECIFIED

-50	-40	30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 - 1°; XXX = .010

HOLE SIZE: 0.599 - .003; 600.999 - .004; 1.000 1.499 - .005

DASH NO	NUMBER	QTY
10	0117-0123	1
	NEXT ASSEMBLY	

ENG SERV R. [illegible] DATE 2/3/83

DRAWN STM DATE 12-1-82

CHECKED

PROJ ENG [illegible] 2/3/83

MANUFACTURING [illegible] 2-3-83

QUALITY ASSUR [illegible] 2-3-83

GOULD biomation

TITLE CRT CABLE ASSEMBLY

SCALE NONE | SIZE C | PART NUMBER 0117-0021 | REV A

CODE K105 | SHEET 1 OF 1

DWG NO 0117-0021 | SH 1 | REV A

KLINGLER K-VEL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	6100-0130-10	SOCKET, CRT		
2									1	6000-0358-08	HOUSING, 20 PIN		
3									6	6000-0357-10	PIN		
4									1	7200-0039-10	MARKER, TIE WRAP		
5													

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL PER ECO 3957	9-16-83	STM	[illegible]
0	PILOT REL PER ERN 309	2/2/83	STM	[illegible]

DASH NO.	NUMBER / NEXT ASSEMBLY	QTY
10	0117-0123	1

		DATE
DWN	STM	12-1-82
CHK		
ENGR	[illegible]	2/3/83
MFG.	[illegible]	2-3-83
Q.A.	[illegible]	2-3-83

LIST OF MATERIAL

CRT CABLE ASSEMBLY

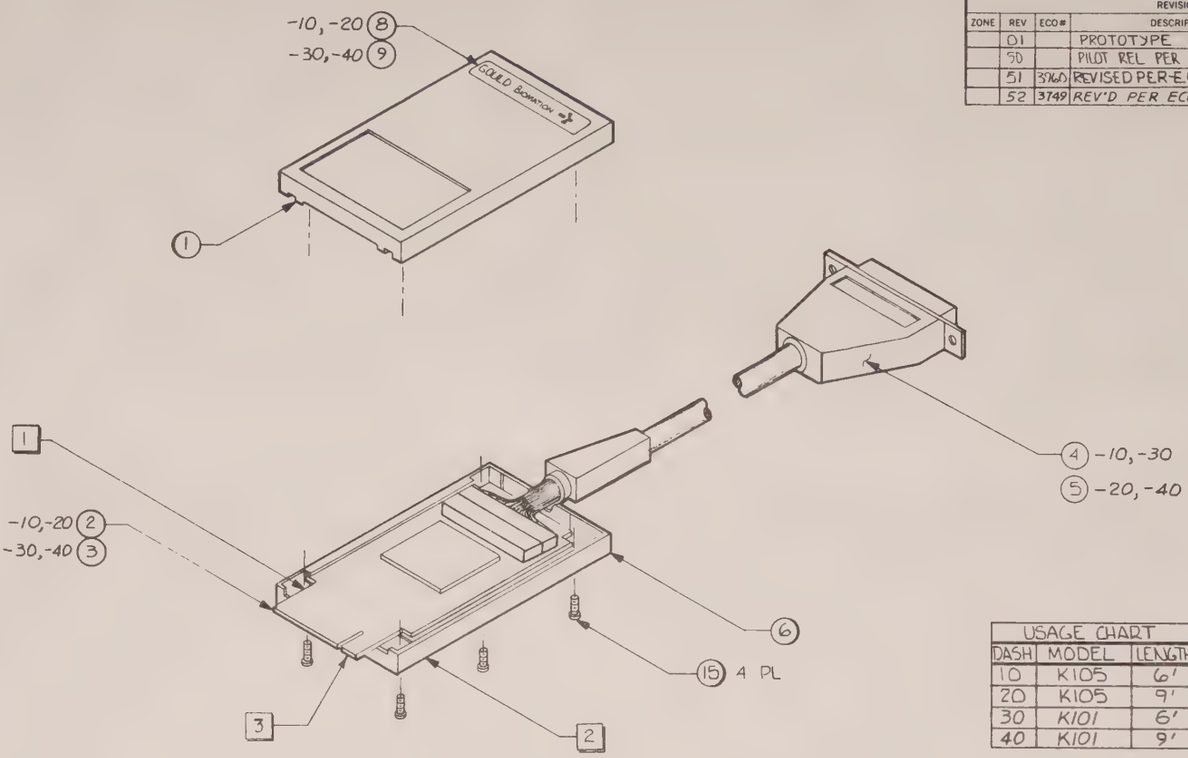
GOULD biomation

B 0117-0021 REV A

MODEL [illegible] SHEET 1 OF 1

KLINGLER K-VEL H.10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	01		PROTOTYPE	STM		1-8-83
	50		PILOT REL PER ERN 335	STM		4-18-83
	51	3960	REVISED PER-E.CO.N°	JWC	DGW	8-24-83
	52	3749	REV'D PER ECO 3749	RTM	DGW 834	2/4/84



USAGE CHART		
DASH	MODEL	LENGTH
10	K105	6'
20	K105	9'
30	K101	6'
40	K101	9'

3 MARK BOTTOM OF CASE LARGE RECTANGULAR RECESS WITH THE FOLLOWING: XXX XX XX XXXXX
MFG N° YEAR WEEK SERIAL N°
0117-0099-XX REV. X
DASH CURRENT REV. LEVEL

2 BAG AND TAG WITH P/N 0117-0099, DASH NO. AND REV. LEVEL.

1 PIN 1 (FARSIDE).

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO	NUMBER NEXT ASSEMBLY	QTY
40	0114-1092	1
40	0114-1091	1
30	0114-1062	1
30	0114-1061	1
20	0117-0174	1
10	0117-0173	1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL X ± 1 ANGLES XX ± .020 ± 1° XXX ± .010
HOLE SIZE 0.599 - .003 .600 .999 - .004 1.000-1.499 - .005
ENG SERV R. Gipson DATE 4/15/83

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
-50 -40 -30 -20 -10			1

DRAWN STM DATE 1-8-83
CHECKED R. Wood 4/19/83
PROJ ENG 5/13/83
MANUFACTURING 5-13-83
QUALITY ASSUR 5/13/83

GOULD biomation
TITLE PROBE SUB ASSY
SCALE NONE SIZE C PART NUMBER 0117-0099 REV 52
CODE K105/K101 SHEET 1 OF 1

DWG NO 0117-0099 SH 1 REV 52

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1						1	1	1	1	0114-0255-10	CASE, PROBE, TOP		
2						/	/	1	1	0117-0213-10	PROBE PWB ASSY, K105		
3						1	1	/	/	0117-0213-20	PROBE PWB ASSY, K101/K102		
4						/	1	/	1	0117-0022-10	POD TO UNIT CABLE 6'		
5						1	/	1	/	0117-0022-20	POD TO UNIT CABLE 9'		
6						1	1	1	1	0114-0255-20	CASE, PROBE, BOTTOM		
7													
8						/	/	1	1	0117-0171-10	LABEL, PROBE POD, K105		
9						1	1	/	/	0114-0264-10	LABEL, PROBE POD, K101/K102		
10													
11													
12													
13													
14													
15						4	4	4	4	7000-0429-20	SCREW 2 x 3/8" LG PH. HD.		

REV	DESCRIPTION	DATE	DWN	CKD
2	REV'D PER ECO 3749	1-30-84	RTM	DGW STM
	REV'D PER ECO 3960	8-25-83	JWC	DGW
0	PILOT REL PER ERN 335	4-18-83	STM	
1	PROTOTYPE	1-8-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
40	0114-1092	1
40	0114-1091	1
30	0114-1062	1
30	0114-1061	1
20	0117-0174	1
10	0117-0173	1

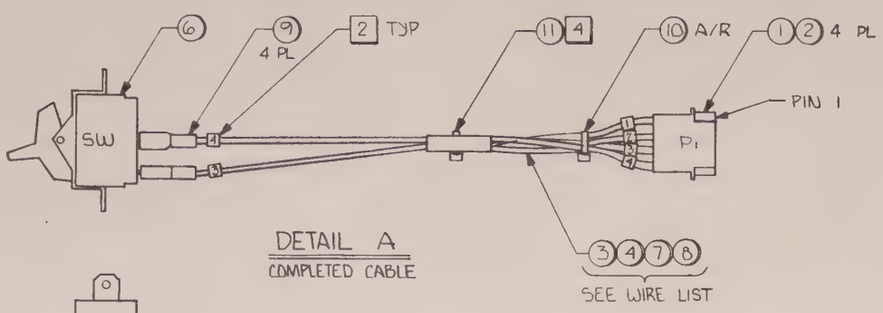
DWN STM DATE 1-8-83
CHK R. Wood 4/22/83
ENGR 7/5/83
MFG 5-13-83
Q.A. 5/13/83

LIST OF MATERIAL
PROBE SUB ASSEMBLY

GOULD biomation
B 0117-0099 REV 52
MODEL K105-K101 SHEET 1 OF 1

KLINGLER K-VEL H-10

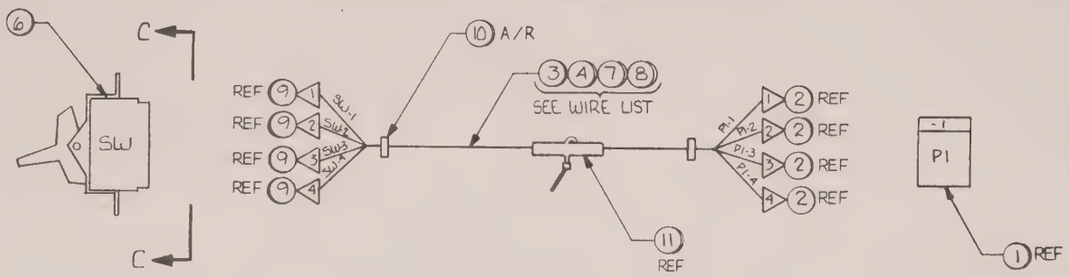
REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 316	STM		1-31-83
	A	3957	PROD REL PER ECO#	STM	DGW	9-16-83



DETAIL A
COMPLETED CABLE

VIEW C-C

WIRE LIST						
WIRE NO.	ITEM NO	FROM	TO	COLOR	AWG	LENGTH
1	8	P1-1	SW-1	WHT/VIO	18	7"
2	3	P1-2	SW-2	WHT/BRN	18	7"
3	4	P1-3	SW-3	BLU/BLK	18	7"
4	7	P1-4	SW-4	WHT/ORN	18	7"



DETAIL B
CABLE SCHEMATIC

5. ◁ TERMINATION TRIANGLE INDICATES WIRE NO.

4 TAG HARNESS WITH ASSY NO 0117-0117-10 AND REV LEVEL AS SHOWN

2 IDENTIFY END OF WIRES WITH DESTINATION AS SHOWN

1. DWG IS TO SCALE + MAY BE USED AS A TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X - 1 ANGLES; XX - .020 - 1°; XXX - .010; HOLE SIZE .599 - .002 / .600 .599 - .864 / 1.000 1.499 - .005

DRAWN	STM	DATE	1-5-83
CHECKED	R. Wood		2-15-83
PROCESS ENG			2-18-83
MANUFACTURING			2-18-83
QUALITY ASSUR			

GOULD biomation

TITLE: CABLE ASSEMBLY POWER SWITCH

SCALE	SIZE	PART NUMBER	REV
	C	0117-0117	A

CODE K105 SHEET 1 OF 1

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	6000-0024-10	CONNECTOR PIN HOUSING	P1	
2									4	6000-0157-10	CONNECTOR PIN		
3									.75	7150-0018-19	WIRE, PVC, 18 AWG, WHT/BRN		
4									.75	7150-0018-37	WIRE, PVC, 18 AWG, BLU/BLK		
5													
6									1	9000-0093-10	POWER SWITCH		
7									.75	7150-0018-20	WIRE, PVC, 18 AWG, WHT/ORG		
8									.75	7150-0018-22	WIRE, PVC, 18 AWG, WHT/VIO		
9									4	6200-0036-10	TERM. FEMALE DISC.		
10									A/R	7200-0008-10	CABLE TIE 4" LNG.		
11									1	7200-0039-10	MARKER TIE WRAP 4" LNG.		

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL PER ECO 3957	9-16-83	STM	DGW
50	PILOT REL PER ERN 316	1-31-83	STM	

DASH NO.	NUMBER	QTY
10	0117-0005	1
	NEXT ASSEMBLY	

DWN	STM	8-24-82
CHK	R. Wood	2-15-83
ENGR		2-18-83
MFG.		2-18-83
Q.A.		

LIST OF MATERIAL
CABLE ASSEMBLY-
POWER SWITCH

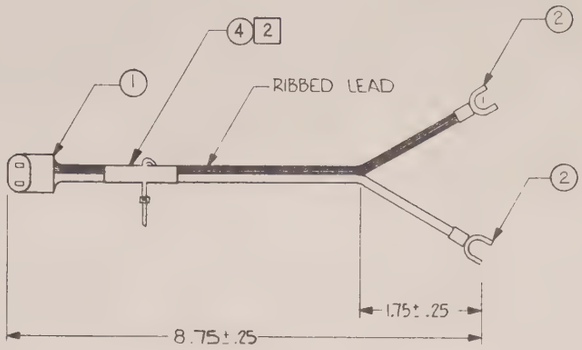
GOULD biomation

B 0117-0117 REV A

MODEL K105 SHEET 1 OF 1

KLINGLER MVEL H10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 316	STM		1-31-83
	A	3957	PROD REL PER ECO#	STM	DGW	9-16-83
	RC	4341	RECORD CHANGE	MW	DGW	2/28/83



2 TAG HARNESS WITH ASSY NO., DASH NO. + REV LEVEL WHERE SHOWN.

1. DRAWING IS TO SCALE AND MAY BE USED AS A TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO	NUMBER NEXT ASSEMBLY	QTY
-10	0117-0006	2

-50	-40	30	-20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX .020 ± .1°, XXX ± .010; ANGLES; HOLE SIZE: 0.599 .003, 600.999 .004, 1.000 1.499 .005

ENG SERV R. Gyson DATE 2/18/83

DRAWN STM	DATE 11-23-82	GOULD biomation
CHECKED R. Wood	2-15-83	TITLE FAN HARNESS ASSY
PROJ ENG	2-18-83	
MANUFACTURING	2-18-83	SCALE 1:1 · SIZE C · PART NUMBER 0117-0124 · REV A
QUALITY ASSUR		CODE K105 · SHEET 1 OF 1

KLINGLER K-VEL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION
1									1	2900-0008-10	FAN CORD	
2									2	6200-0054-10	FORK, LUG 14-16 AWG	
3												
4									1	7200-0039-10	MARKER, TIE WRAP 4" LG	

REV	DESCRIPTION	DATE	DWN	CKD
C	RECORD CHANGE # 4341	2/28/83	MW	DGW
A	PROD REL PER ECO# 3957	9-16-83	STM	DGW
50	PILOT REL PER ERN 316	1-31-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117-0006	2

		DATE
DWN	STM	11-23-82
CHK	R Wood	2-15-83
ENGR		2-18-83
MFG.		2-18-83
Q.A.		

LIST OF MATERIAL

FAN HARNESS ASSEMBLY

GOULD biomation

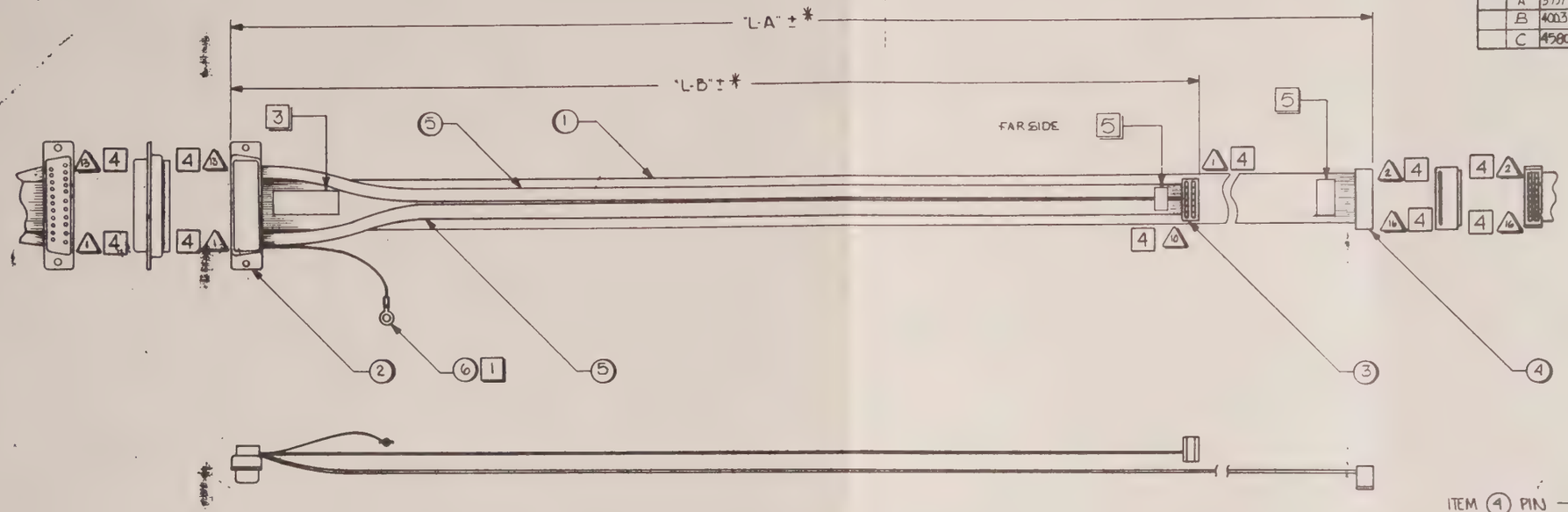
B 0117-0124 REV A

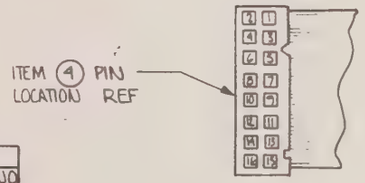
MODEL K105 SHEET 1 OF 1

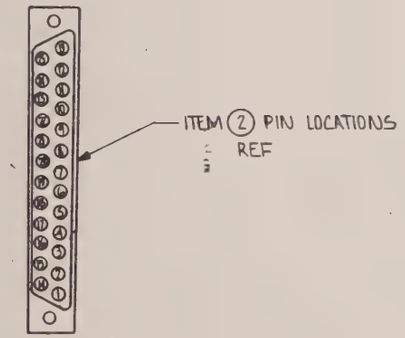
KLINGLER K-VEL H 10

DWG. NO. 0117-0128 SH 1 REV C

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	03		REVISED	STM		1-31-83
	04		REVISED N/A'S	STM		2-2-83
	05		REVISED PIN OUTS ADDED DETAILS	STM		2-11-83
	06		REVISED ENG. ERROR	STM		2-14-83
	50		PILOT REL PER ERN 333	STM		3-30-83
	51	3896	REVISED PER ECO	MW	DGW	7-14-83
	52	3919	REVISED PER ECO No	JWC	DGW	8-15-83
	A	3957	PROD REL PER ECO#	STM	DGW	9-16-83
	B	4003	REVISED PER ECO No	JWC	DGW	10-18-83
	C	4580	PER ECO	[illegible]	[illegible]	7/5/84





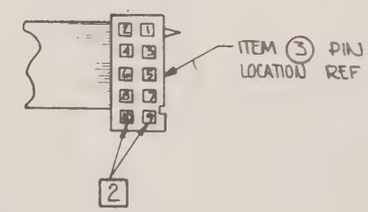


DASH No	"L – A" LENGTH	"L – A" DEST	"L – B" LENGTH	"L – B" DEST
01	40"	A CLK	20"	J22
02	40"	B CLK	20"	J24
03	40"	C CLK	20"	J21
04	40"	D CLK	20"	J23
05	40"	A F-8	20"	J25
06	40"	B F-8	20"	J26
07	40"	C F-8	20"	J27
08	40"	D F-8	20"	J28

* NOTE: LENGTHS MAY BE ROUNDED TO THE NEXT CLOSEST "FLAT SECTION"

WIRE LIST

CONN ITEM NO.	PIN NO.	COLOR	PIN NO.	CONN. ITEM NO
2	1	GREEN	—	6
	14	BIEGE	8	3
	2	YEL	7	3
	15	BIEGE	6	3
	3	ORN	5	3
	16	BIEGE	16	4
	4	GRAY	15	4
	17	BIEGE	14	4
	5	PURPLE	13	4
	18	BIEGE	12	4
	6	BLUE	11	4
	19	BIEGE	10	4
	7	GRN	9	4
	20	BIEGE	8	4
	8	YEL	7	4
	21	BIEGE	6	4
	9	ORN	5	4
	22	BIEGE	4	4
	10	RED	3	4
	23	BIEGE	2	4
	11	BRN	1	4
	24	BIEGE	4	3
	12	RED	3	3
	25	BIEGE	2	3
2	13	BRN	1	3
		N/C		3
		N/C		3



5 LABEL DESTINATION OF CABLES PER P/N CHART

4. △ DENOTES PIN NO. ON CONNECTOR

3. IDENTIFY WITH ASSY NO. 0117-0128, DASH NO. + REV LEVEL

2 PINS 9 + 10 ARE NO-CONNECTION

1 REMOVE 1ST CONDUCTOR (BIEGE) THEN PEEL + CUT 2ND CONDUCTOR (GRN) TO LENGTH OF 4" AND INSTALL ITEM 6.

NOTES: UNLESS OTHERWISE SPECIFIED

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .010 ± 1°; XXX = .010

HOLE SIZE: 0 599 - 003; 600 999 - 004; 1 000 1 499 - 005

DRAWN STM DATE 1.14.83

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSUR

ENG SERV DATE

GOULD Instruments Division Santa Clara Operations

TITLE CABLE KIT, MAIN CHANNELS

SCALE | SIZE D | PART NUMBER 0117-0128 | REV C

MODEL K105 | SHEET 1 OF 1

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

ITEM	QUANTITY PER ASSEMBLY								PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
	...	-08	-07	-06	-05	-04	-03	-02	-01				
1		3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5'	7100-0068-08	RIBBON CABLE, 8 PAIRS		
2		1	1	1	1	1	1	1	1	6000-0559-10	CONN. 25 PIN		
3		1	1	1	1	1	1	1	1	6000-0551-20	CONN, 10 PIN SOCKET		
4		1	1	1	1	1	1	1	1	6000-0352-20	CONN. 16 CONTACT SKT.		
5		2'	2'	2'	2'	2'	2'	2'	2'	7100-0068-05	RIBBON CABLE, 5 PAIRS		
6		1	1	1	1	1	1	1	1	6200-0024-10	TERMINAL, RING TONGUE RED		
7													
8													
9													
10													

REV	DESCRIPTION	DATE	DWN	CKD
C	PER ECO 4580	7-2-84	[illegible]	[illegible]
	SEE HISTORY			

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-08	0117-0005	1
-07		1
-06		1
-05		1
-04		1
-03		1
-02		1
-01	0117-0005	1

		DATE
DWN	STM	1-12-83
CHK	[signature]	1/13/83
ENGR	[signature]	1/13/83
MFG.	[signature]	1-13-83
Q.A.	[signature]	1-14-83

LIST OF MATERIAL

CABLE KIT,
MAIN CHANNELS

GOULD biomation

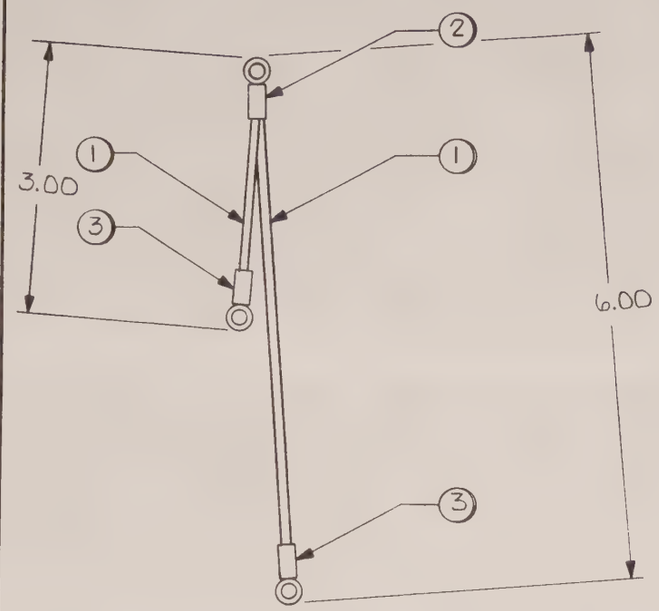
B | 0117-0128 | REV C

MODEL K10S | SHEET 1 OF 1

KLINGLER M-VEL H-10

DWG. NO. 0117-0133 | SH 1 | REV A

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
01		PROTOTYPE	STM		2-4-83
50		PILOT REL. PER ERN 322			2-8-83
51	3872	REVISED PER ECO#2	SWC	DGW	7-7-83
A	3957	PROD. REL PER ECO#	STM	DGW	9-16-83



2. BAG & TAG WITH P/N 0117-0133 DASH NO AND REV LEVEL.
1. DRAWING IS TO SCALE & MAY BE USED AS TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES, EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL
X ± .1 ANGLES
XX ± .020 ± 1°
XXX ± .010

HOLE SIZE
0 .599 + .003
.600 .999 + .004
1.000 1.499 + .005

DRAWN	STM	DATE 2-4-83
CHECKED	R. Wood	2/28/83
ENGINEERING		3/25/83
MANUFACTURING		3-25-83
QUALITY ASSUR		3-25-83
ENG SERV		DATE 3/25/83

GOULD biomation

TITLE: CHASSIS GND CABLE

SCALE	SIZE	PART NUMBER	REV
1:1	B	0117-0133	A

CODE K105 | SHEET 1 OF 1

DASH NO.	NUMBER	QTY
10	0117-0003	1
	NEXT ASSEMBLY	

KLINGLER K-VEL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									.75'	7100-0020-10	WIRE STRND 20 GA. BLK		
2									1	6200-0030-10	LUG TERM., TERM RING. TOUNGE BLUE		
3									2	6200-0025-10	LUG TERM., TERM RING. TOUNGE RED		

REV	DESCRIPTION	DATE	DWN	CKD
	PROD. REL PER ECO 3957	9-16-83	STM	DGW
	REVISED PER ECO 3872	7-7-83	SWC	DGW
0	PILOT REL. PER ERN 322	2-8-83	STM	

DASH NO.	NUMBER	QTY
10	0117-0003	1
	NEXT ASSEMBLY	

		DATE
DWN	STM	2-4-83
CHK	R. Wood	3/25/83
ENGR		3/25/83
MFG.		3-25-83
Q.A.		3-25-83

LIST OF MATERIAL

CHASSIS GND CABLE

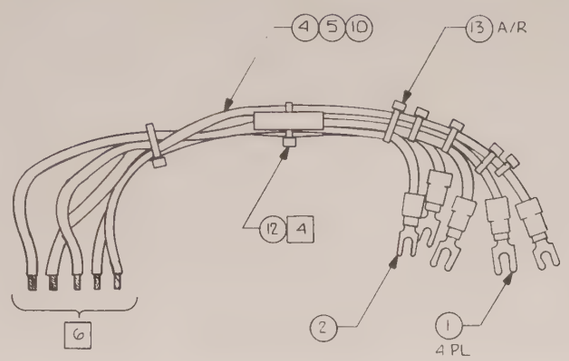
GOULD biomation

B | 0117-0133 | REV A

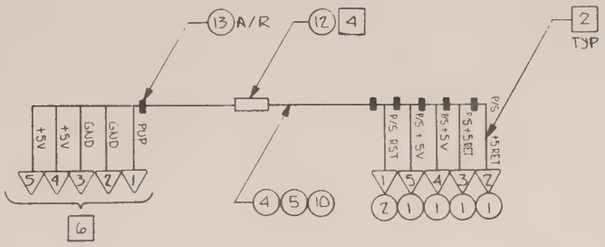
MODEL K105 | SHEET 1 OF 1

KLINGLER K-VEL H10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 322	STM		3-23-83
	51	3873	REVISED PER ECO	JWC	DGW	7-12-83
	A	3957	PROD. REL PER ECO # 4	STM	DGW	9-16-83



WIRE NO.	FROM	TO	AWG	COLOR	LENGTH
1	P/S RST	PUP	16	WHT	6.5"
2	P/S+5V RET	GND	12	BLK	7.5"
3	P/S+5V RET	GND	12	BLK	7.5"
4	P/S+5V	+5V	12	RED	7.5"
5	P/S+5V	+5V	12	RED	7.5"



6 STRIP INSULATION .25"

5. ▽ TERMINATION TRIANGLE INDICATES WIRE NO.
○ CIRCLE INDICATES ITEM NO. ON PARTS LIST.

4 TAG HARNESS WITH ASSY NO. 0117-0144 DASH NO. AND REV. LEVEL AS SHOWN.

3. TIP OF TERMINATION TRIANGLE DENOTES END OF CUT WIRE BEFORE LUGGING.

2 IDENTIFY PLUGS AND ENDS OF WIRES WITH DESTINATION AS SHOWN.

1. DRAWING IS TO SCALE AND MAY BE USED AS A TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO	NUMBER	QTY
10	0117-0145	1
	NEXT ASSEMBLY	

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X - ± ANGLES; XX - .020 ± 1°; XXX - .010
HOLE SIZE: 0.599 - .003; 600.999 - .004; 1.000-1.499 - .005

DRAWN	STM	DATE 5-8-83
CHECKED	R. Wood	3/23/83
PROJ. ENG.	[signature]	3/23/83
MANUFACTURING	[signature]	3-23-83
QUALITY ASSUR	[signature]	3-23-83
ENG SERV.	R. Gipson	DATE 3/23/83

GOULD biomation

TITLE: HARNESS, MOTHER BOARD

SCALE	SIZE	PART NUMBER	REV
1:1	C	0117-0144	A

CODE K105 SHEET 1 OF 1

KLINGLER K-VEL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									4	6200-0055-10	FORK LUG 10-12 AWG		
2									1	6200-0054-10	FORK LUG 14-16 AWG		
3													
4									1.25'	7150-0012-02	WIRE 12 AWG RED		
5									1.25'	7150-0012-10	WIRE 12 AWG BLK		
6													
7													
8													
9													
10									.6'	7150-0016-09	WIRE 16 AWG WHT		
11													
12									1	7200-0039-10	MARKER, TIE WRAP 4" LNG		
13									A/R	7200-0008-10	CABLE TIE 4" LNG		

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL PER ECO 3957	9-16-83	STM	DGW
51	REVISED PER ECO 3873	7-12-83	JWC	DGW
50	PILOT REL PER ERN		STM	

DASH NO.	NUMBER / NEXT ASSEMBLY	QTY
10	0117-0045	1

		DATE
DWN	STM	1-20-83
CHK	R Wood	3/23/83
ENGR	[signature]	3/23/83
MFG.	[signature]	3-23-83
Q.A.	[signature]	3-23-83

LIST OF MATERIAL
MOTHERBOARD
HARNESS

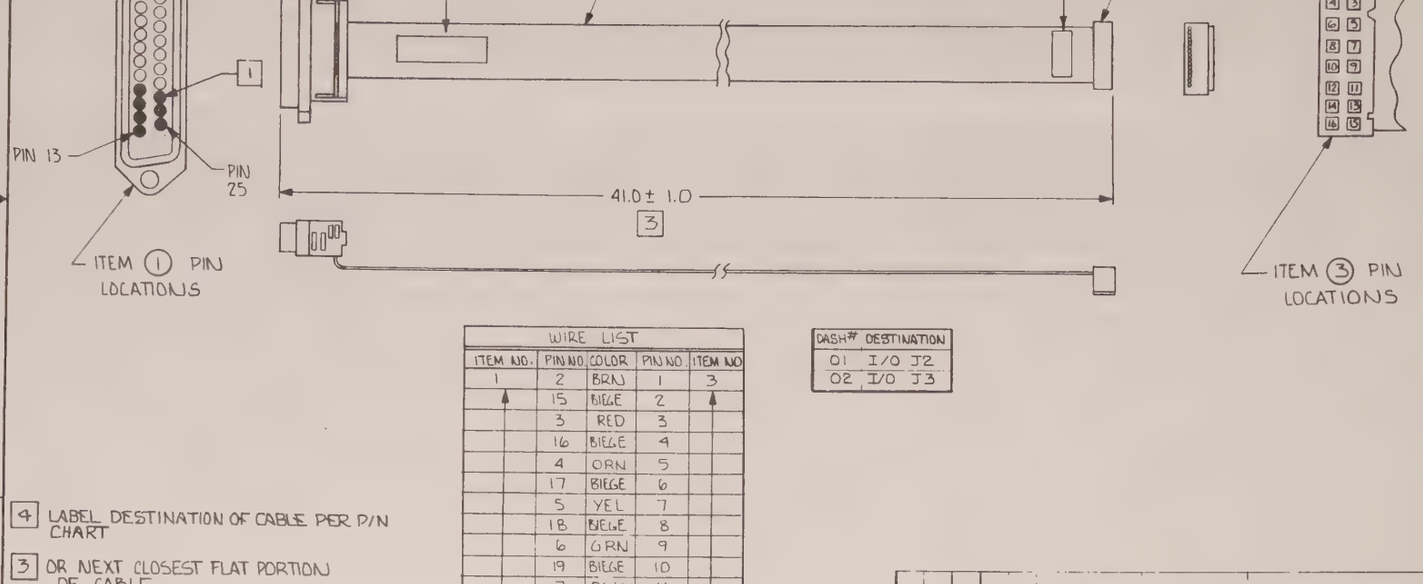
GOULD biomation

B 0117-0144 REV A

MODEL K105 SHEET 1 OF 1

KLINGLER K-VEL H 10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	01		PROTOTYPE	STM		2-4-83
	50		PILOT REL PER ERN 333	STM	[signature]	3-30-83
	51	3768	REV'D PER ECO	MW	DGW	5/24/83
	A	3759	PROD REL PER ECO# [signature]	STM	DGW	9-16-83
	B	4003	REVISED PER ECO#	JWC	DGW [signature]	10/18/83



WIRE LIST				
ITEM NO.	PIN NO.	COLOR	PIN NO.	ITEM NO.
1	2	BRN	1	3
	15	BIEGE	2	
	3	RED	3	
	16	BIEGE	4	
	4	ORN	5	
	17	BIEGE	6	
	5	YEL	7	
	18	BIEGE	8	
	6	GRN	9	
	19	BIEGE	10	
	7	BLU	11	
	20	BIEGE	12	
	8	VIO	13	
	21	BIEGE	14	
	9	GRY	15	
1	22	BIEGE	16	3

DASH#	DESTINATION
01	I/O J2
02	I/O J3

4 LABEL DESTINATION OF CABLE PER P/N CHART

3 OR NEXT CLOSEST FLAT PORTION OF CABLE.

2. IDENTIFY WITH ASSY NO. 0117-0157 DASH NO. AND REV. LEVEL.

1 PINS NO 1, 14, 10, 23, 11, 24, 12, 25 AND 13 ON CONN. ITEM 1 ARE NO CONNECTION

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO	NUMBER	QTY
02	0117-0120	1
01	0117-0120	1

NEXT ASSEMBLY

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL X = 1 ANGLES XX = .020 ± 1° XXX = .010
HOLE SIZE 0.599 - .003 .600 .999 - .004 1.000 1.499 - .005

ENG SERV R [signature] DATE 4/13/83

	DATE
DRAWN STM	2-14-83
CHECKED [signature]	4/13/83
PROD ENG [signature]	4/13/83
MANUFACTURING [signature]	4-13-83
QUALITY ASSUR [signature]	4-14-83

GOULD biomation

TITLE HARNESS ASSY, RS232 C, K105

SCALE	SIZE	PART NUMBER	REV
NONE	C	0117-0157	B

CODE K105 SHEET 1 OF 1

KLINGLER K-VEL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	02	01	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1								1	1	6000-0559-10	CONN. 25 PIN, SOCKET		
2								3'	3'	7100-0068-08	RIBBON CABLE, 8 PAIRS		
3								1	1	6000-0352-10	CONN. 16 CONTACT SOCKET		

REV	DESCRIPTION	DATE	DWN	CKD
B	REV'D PER ECO 4003	10/18/83	JWC	DGW
A	PROD. REL PER ECO 3757	9-16-83	STM	DGW
1	REV'D PER ECO 3768	5/23/83	MW	DGW
50	PILOT REL PER ERN 333	3-30-83	[signature]	[signature]
01	PROTOTYPE	2-14-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-02	0117-0120	1
-01	0117-0120	1

		DATE
DWN	STM	2-14-83
CHK	[signature]	4/13/83
ENGR	[signature]	4/13/83
MFG.	[signature]	4-13-83
Q.A.	[signature]	4-14-83

LIST OF MATERIAL

HARNESS ASSY
RS232 C, K105

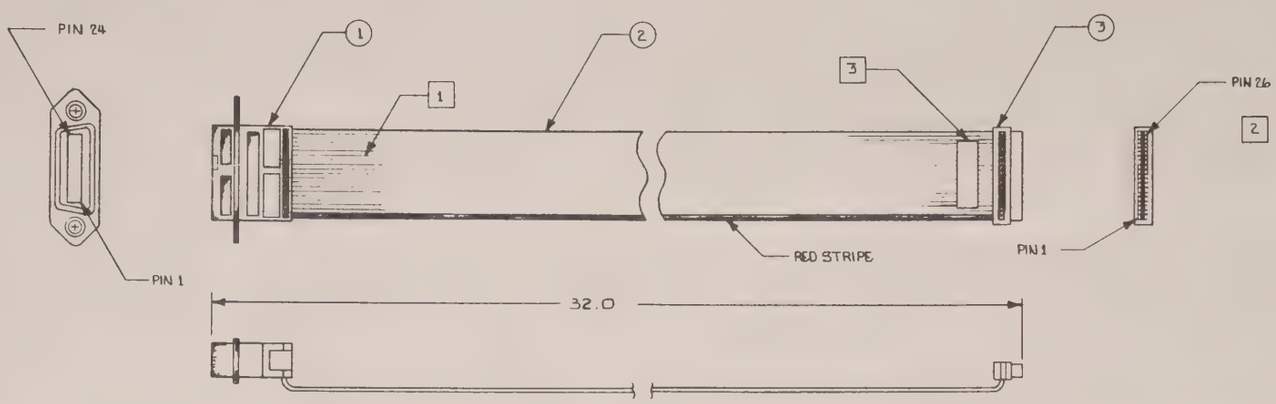
GOULD biomation

B 0117-0157 REV B

MODEL K105 SHEET 1 OF 1

KLINGLER K-VEL H-10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	B	4003	REVISED PER E.C.O N°			
	BRC	4573	REVISED PER E.C.O N° 6-7-84	JWC	DGW 6-8-84	



NOTES: UNLESS OTHERWISE SPECIFIED

1. IDENTIFY WITH ASSY NO. 0117-0158 DASH NO. AND REV LEVEL.
2. PINS 25 AND 26 OF ITEM 3 ARE NO CONNECTION
3. LABEL DESTINATION "I70 J5" WHERE SHOWN

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					
				PARTS LIST	
-10	0117-0120	1			
DASH NO.	NEXT ASSY	USED ON			
FIRST APPLICATION					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX ±
XXX ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN J.W.CARROLL	6-7-84
CHECKED	
PROJ ENG	

GOULD Electronics

TITLE: HARNESS ASSY I.E.E.E. 488 K105

SIZE C | DWG NO 0117-0158 | REV B

SCALE | MODEL K105 | SHEET 1 OF 1

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	6000-0304-10	CONN 24 PIN		
2									3'	7100-0090-10	CABLE, FLAT 24 CONDUCTOR		
3									1	6000-0403-10	CONN. 26 PIN, FLAT CABLE		
4													

REV	DESCRIPTION	DATE	DWN	CKD
BRC	REV'D PER E.C.O 4573	6-7-84	JWC	DGW
B	REV'D PER E.C.O 4003	9-16-83	JWC	DGW
A	PROD REL PER ECO 3957	9-6-83	SJM	DGW
51	REVISED E.C.O 3930	8-17-83	JWC	DGW
50	PILOT REL PER ERO 333	5-30-83	SJM	
01	PROTOTYPE	2-14-83		

DASH NO.	NUMBER	QTY
10	0117-0120	1
	NEXT ASSEMBLY	

		DATE
DWN	RJM	2-14-83
CHK		4/7/83
ENGR		4/13/83
MFG.		4-13-83
Q.A.		4-14-83

LIST OF MATERIAL

HARNESS ASSY
I.E.E.E 488 K105

GOULD biomation

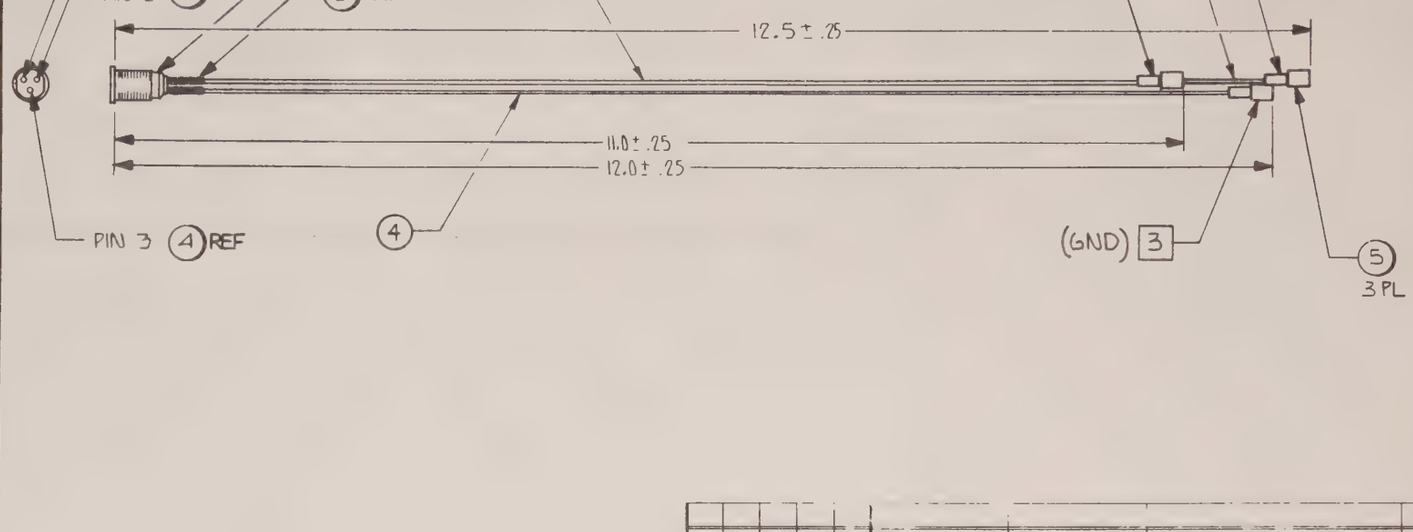
B | 0117-0158 | REV B

MODEL K105 | SHEET 1 OF 1

KLINGLER K-VELL H10

DWG NO. 0117-0165 | SH 1 | REV A

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
01		PROTOTYPE	STM		2-4-83
50		PILOT REL	[illegible]		
A	3957	PROD. REL PER ECO #	STM	DGW	9-16-83



3 IDENTIFY END OF WIRES WITH DESTINATION AS SHOWN.

2. BAG & TAG WITH P/N 0117-0165 DASH NO. AND REV LEVEL.

1. DWG IS TO SCALE & MAY BE USED AS A TEMPLATE.

NOTES UNLESS OTHERWISE SPECIFIED

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117-0170	2

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE: DIMENSIONAL X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°; HOLE SIZE 0.599 - .003, 600.999 - .004, 1.000 1.499 - .005

ENG. SERV. R. Gipson — DATE 3/23/83

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DRAWN STM — DATE 2-4-83

CHECKED R. Wood — 2/28/83

PROJ. ENG. [signature] — 3/25/83

MANUFACTURING [signature] — 3-23-83

QUALITY ASSUR [signature] — 3-23-83

GOULD biomation

TITLE: HARNESS ASSY ± 5V

SCALE 1:1 | SIZE B | PART NUMBER 0117-0165 | REV A

CODE K105 | SHEET 1 OF 1

KLINGLER K-VEL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	6000-0181-10	CONN., 3 PIN PLUG (LEMA)		
2									1'	7150-0024-02	WIRE STRAND, 24 GA. RED		
3									1'	7150-0024-06	WIRE STRAND, 24 GA. BLUE		
4									1'	7150-0024-10	WIRE STRAND, 24 GA. BLK		
5									3	6200-0035-10	TERMINAL, FEMALE DISCONNECT		
6									1.5"	7200-0001-10	TUBING HEAT SHRINK 3/32"		

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD. REL PER ECO# 3957	9-16-83	JM	DGW
50	PILOT REL		JM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117-0120	2

DWN STM — DATE 2-4-83

CHK [signature] — 3-25-83

ENGR [signature] — 3/25/83

MFG. [signature] — 3-25-83

Q.A. [signature] — 3-25-83

LIST OF MATERIAL

HARNESS ASSY ± 5V

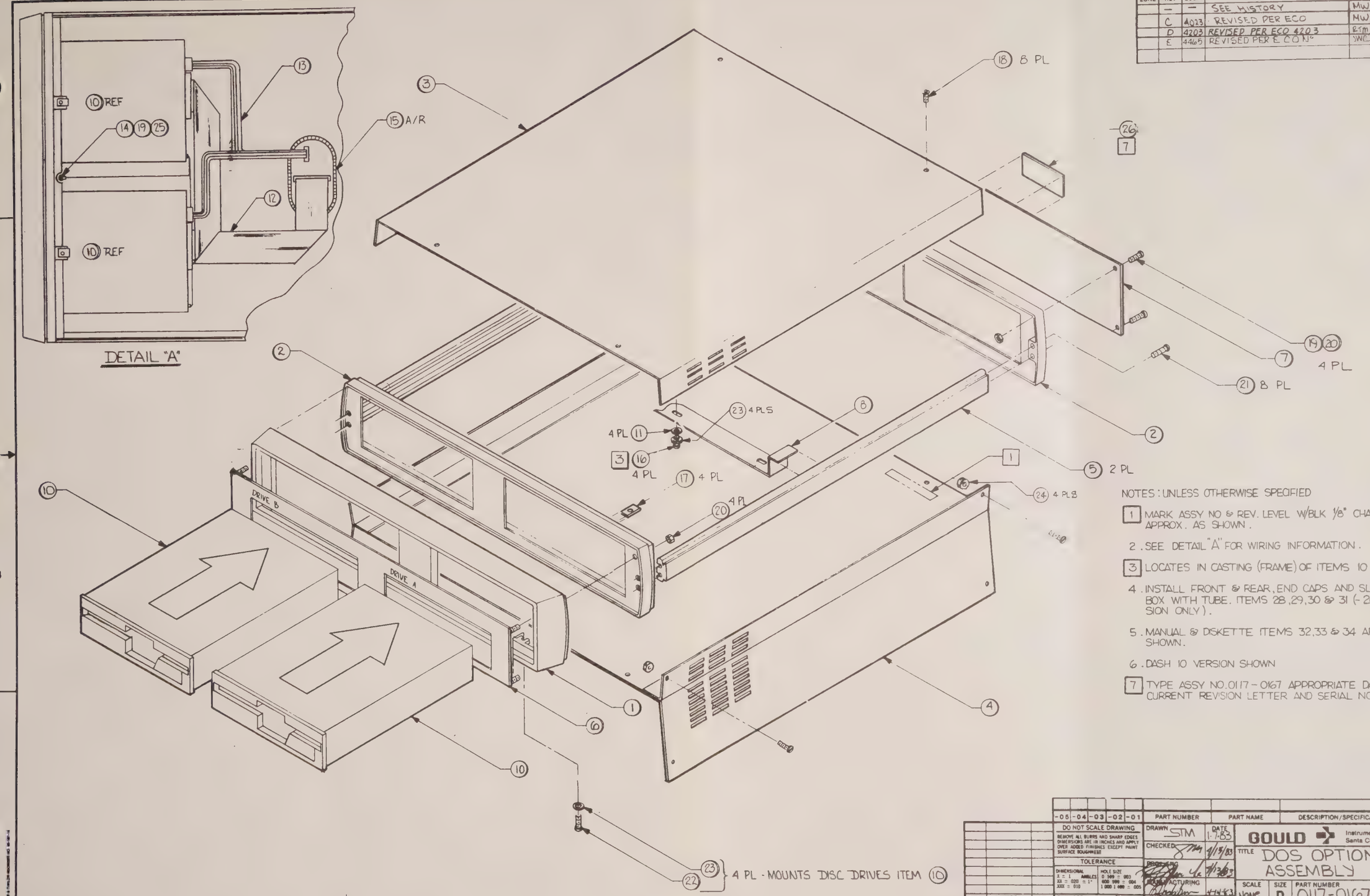
GOULD biomation

B | 0117-0165 | REV A

MODEL K105 | SHEET 1 OF 1

KLINGLER K-VEL H-10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	—	—	SEE HISTORY	MW		
	C	4023	REVISED PER ECO	MW	[illegible]	[illegible]
	D	4203	REVISED PER ECO 4203	RTM	[illegible]	5/9/84
	E	4465	REVISED PER E.C.O. N°	JWC	[illegible]	4/6/84



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSY NO & REV. LEVEL W/BLK 1/8" CHARACTERS APPROX. AS SHOWN.
2. SEE DETAIL "A" FOR WIRING INFORMATION.
3. LOCATES IN CASTING (FRAME) OF ITEMS 10 & 11
4. INSTALL FRONT & REAR, END CAPS AND SLIDE INTO BOX WITH TUBE. ITEMS 28, 29, 30 & 31 (-20 VERSION ONLY).
5. MANUAL & DISKETTE ITEMS 32, 33 & 34 ARE NOT SHOWN.
6. DASH 10 VERSION SHOWN
7. TYPE ASSY NO. 0117-0167 APPROPRIATE DASH NO., CURRENT REVISION LETTER AND SERIAL NO.

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: 0.599 ± .003; 600.999 ± .004; 1.000 1.499 ± .005

DRAWN STM	DATE 1-7-83	GOULD Instruments Division Santa Clara Operations
CHECKED [signature]	4/13/83	TITLE DOS OPTION ASSEMBLY
PROJ. ENG [signature]	4/13/83	
MANUFACTURING [signature]	4-14-83	SCALE NONE · SIZE D · PART NUMBER 0117-0167 · REV E
QUALITY ASSUR [signature]	4-14-83	MODEL K105 · SHEET 1 OF 1

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG SERV R. [signature] DATE 9/13/83

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
28								1	—	8400-0017-10	END CAP FRONT		
29								1	—	8400-0018-10	END CAP REAR		
30								1	—	8400-0019-10	ACCESSORY TUBE		
31								1	—	8400-0020-10	SHIPPING BOX		
32								—	1	0117-0256-10	DOS MANUAL		
33													
34								1	—	0117-0304-10	INSTR. SHEET		
35													
36								1	—	0117-0167-10	DOS OPTION		

NOTES	LIST OF MATERIAL	GOULD biomation
	DOS OPTION ASSEMBLY	B 0117-0167 REV E MODEL K105 SHEET 2 OF 2

KLINGLER K-VEL H10

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1								—	1	0114-0462-30	BEZEL, FRONT		
2								—	2	0114-0463-30	BEZEL, REAR		
3								—	1	0114-0466-30	COVER, TOP		
4								—	1	0114-0467-30	COVER		
5								—	2	0114-0465-30	SIDE RAIL		
6								—	1	0114-0470-40	PANEL FRONT		
7								—	1	0117-0169-30	PANEL REAR		
8								—	1	0114-0441-10	BRKT FLOPPY DISK SUPPORT		
9													
10								—	2	7500-0003-10	FLOPPY DISK #5		
11								—	4	7084-0004-10	INT. STAR LOCKWASHER #4		
12								—	1	0117-0164-10	CABLE ASSY I/O TO FLOPPY		
13								—	1	0117-0170-10	HARNESS ASSY, DOS PWR		
14								—	1	0114-0485-10	CABLE ASSY, FLOPPY GND		
15								—	AR	7200-0044-20	CONTINUOUS GROMMET		
16									4	7000-0463-08	SCR. 3MM X 8 MM L PHIL. HD		
17								—	4	7000-0334-10	HARDWARE "U" SPEED NUT, FASTENER	#6-32	
18								—	8	7021-2632-12	SCREW FLT HD PHP S.ST 6-32X3/8LG		
19								—	5	7011-0632-16	SCREW PH PAN HD	#6-32 X .50 LG.	
20								—	8	7071-0632-00	KEPNUT #6		
21								—	8	7012-0600-20	SCREW	#6-32 X .62 LG.	
22								—	4	7000-0463-12	SCREW 3MM X 12 MM	PHILIPS HD 3X 12 DIN 7985	
23								—	8	7082-1004-00	WASHER, FLAT	#4 L.P	
24								—	4	7072-1632-00	HEX NUT NYLON LOCKING	#6-32	
25								—	1	7086-0006-00	STAR WASHER #6		
26								—	1	63030040	LABEL, MODEL		
27								—	1	0117-0261-10	KIOS STORAGE OPERATING SYSTEM	CUSTOMER DISKETTE	

REV	DESCRIPTION	DATE	DWN	CKD
52	REV'D PER ECO 3818	6/1/83	MW	DGW
A	PRINT REL 3957	9/8/83	DGW	DGW
B	REV'D PER ECO 4099	11-29-83	DGW	DGW
C	REV'D PER ECO 4023	12/6/83	MW	DGW
D	REV'D PER ECO 4203	3/9/84	RTM	DGW
E	REV'D PER ECO 4265	6/7/84	JWC	DGW

DASH NO.	N.A. NUMBER NEXT ASSEMBLY	QTY

		DATE
DWN	STM	1-7-83
CHK		1/13/83
ENGR		1/13/83
MFG		4-4-83
Q.A		4-14-83

LIST OF MATERIAL
DOS OPTION ASSEMBLY

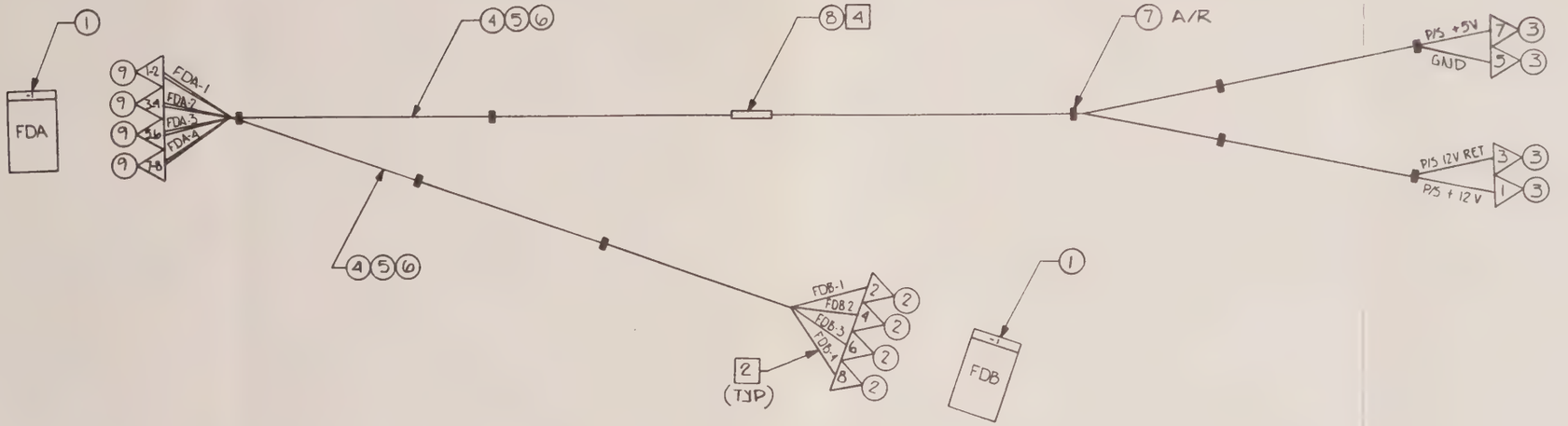
GOULD biomation

B 0117-0167 REV E

MODEL K105 SHEET 1 OF 2

KLINGLER K-VEL H10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	02		REVISED + REDRAWN	STM		2-10-83
	50		PILOT REL PER ERN 333	STM	[illegible]	3-30-83
	A	3955	PROD REL PER ECO No [illegible]	JWC	[illegible]	[illegible]



WIRE NO.	FROM	TO	AWG	COLOR	LENGTH
1	FDA-1	P/S +12V	20	BRN	21"
2	FDA-1	FDB-1	20	BRN	12"
3	FDA-2	P/S 12V RET	20	BLK	21"
4	FDA-2	FDB-2	20	BLK	12"
5	FDA-3	GND	20	BLK	21"
6	FDA-3	FDB-3	20	BLK	12"
7	FDA-4	P/S +5V	20	RED/BLK	21"
8	FDA-4	FDB-4	20	RED/BLK	12"

5. ◁ TERMINATION TRIANGLE INDICATES WIRE NO. ◯ INDICATES ITEM NO. ON PARTS LIST.

[4] TAG HARNESS WITH PART NO. 0117-0170 DASH NO. AND REV LEVEL AS SHOWN.

3. TIP OF TERMINATION TRIANGLE DENOTES END OF CUT WIRE BEFORE LUGGING.

[2] IDENTIFY END OF WIRES WITH DESTINATION AS SHOWN.

1. DWG IS TO SCALE AND MAYBE USED AS A TEMPLATE.

NOTES: UNLESS OTHERWISE SPECIFIED

-06	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± 1°; XXX = .010

HOLE SIZE: 0 .599 - .003; .600 .999 - .004; 1.000 1.499 - .005

DASH NO	NUMBER	QTY
10	0117-0167	1
	NEXT ASSEMBLY	

ENG SERV [illegible] DATE 4/13/83

DRAWN STM DATE 2-10-83

CHECKER [illegible] 4/13/83

PROJ ENG [illegible] 4/13/83

MANUFACTURING [illegible] 4-13-83

QUALITY ASSUR [illegible] 4-14-83

GOULD Instruments Division Santa Clara Operations

TITLE: HARNESS ASSY, DOS POWER

SCALE 1:1 | SIZE D | PART NUMBER 0117-0170 | REV A

MODEL K105 | SHEET 1 OF 1

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION
1									2	6100-0062-10	SOCKET 4 PIN	
2									4	6000-0185-10	CONN. SOCKET, (18-24 GA)	
3									4	6200-0035-10	TERMINAL, FEMALE DISCONNECT	
4									6'	7150-0020-10	WIRE 20 AWG BLK	
5									3'	7150-0020-01	WIRE 20 AWG BRN	
6									3'	7150-0020-34	WIRE 20 AWG RED/BLK	
7									A/R	7200-0008-10	CABLE TIE 4" LONG	
8									1	7200-0039-10	MARKER, TIE WRAP 4" LONG	
9									4	6000-0185-20	CONN. SOCKET, (14-20 AWG)	
10												

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL 3755	9/15/83	[illegible]	DGW
50	PILOT REL PER ERN 333	3-30-83	STM	[illegible]
01	PROTOTYPE	2-7-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117-0167	1

		DATE
DWN	STM	2-7-83
CHK	[illegible]	4/13/83
ENGR	[illegible]	4/12/83
MFG.	[illegible]	4-13-83
Q.A.	[illegible]	4-14-83

LIST OF MATERIAL

HARNESS ASSY
DOS POWER

GOULD biomation

B 0117-0170

MODEL K105 SHEET 1 OF 1

KLINGLER K-VEL H-10

DRAWING NUMBER

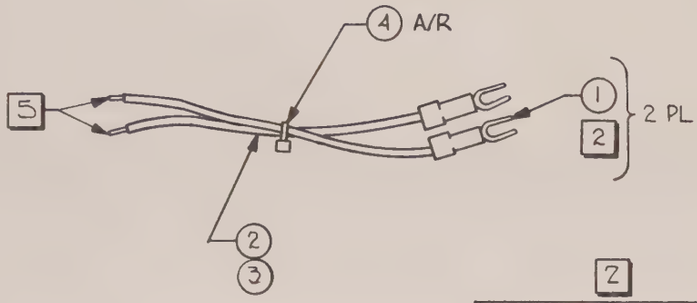
PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 07BAR

DRAWING NUMBER

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 07BAR

DWG. NO. 0117-0221 | SH 1 | REV A

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50		PILOT REL PER ERN 309	STM		2-1-83
A	3957	PROD REL PER ECO N°	JWC	DWJ	9/14/83



[2]

WIRE NO	FROM	TO	AWG	COLOR	LENGTH
1	P15-5.2V	-5.2V	16	BRN	4.0"
2	P15 5.2V RET	5.2V RET	16	BLK	4.0"

[5] STRIP INSULATION .25"

4. MANUFACTURE IN ACCORDANCE WITH WORKMANSHIP STD. B7000012.
3. BAG AND TAG WITH P/N 0117-0221, DASH NO AND REV LEVEL.
[2] IDENTIFY PLUGS AND END OF WIRES WITH DESTINATION AS SHOWN.
1. DRAWING IS TO SCALE AND MAY BE USED AS A TEMPLATE.

NOTES: UNLESS OTHERWISE SPECIFIED

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1, XX ± .020, XXX ± .010; ANGLES ± 1°
HOLE SIZE: 0 599 + .003, 600 999 + .004, 1.000 1.499 + .005

DRAWN	DATE
STM	2-1-83
CHECKED	
PROJ. ENG.	4/3/83
MANUFACTURING	2-3-83
QUALITY ASSUR.	2-3-83

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TITLE MOTHER BOARD CABLE 5.2 V

SCALE	SIZE	PART NUMBER	REV
1:1	B	0117-0221	A

CODE K105 SHEET 1 OF 1

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117-0045	1

ENG SERV. R Gipson DATE 2/3/83

KLINGLER K-VEL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									2	6200-0054-10	FORK LUG 14-16 AWG		
2									.5'	7150-0016-01	WIRE 16 AWG BRN		
3									.5'	7150-0016-10	WIRE 16 AWG BLK		
4									A/R	7200-0008-10	CABLE TIE		

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL 3957	9/14/83	JWC	DWJ
D	PILOT REL PER ERN 309	2-1-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117-0045	1

DWN	STM	DATE 2-1-83
CHK		
ENGR		2/3/83
MFG.		2-3-83
Q.A		2-3-83

LIST OF MATERIAL
MOTHER BOARD CABLE 5.2 V

GOULD biomation

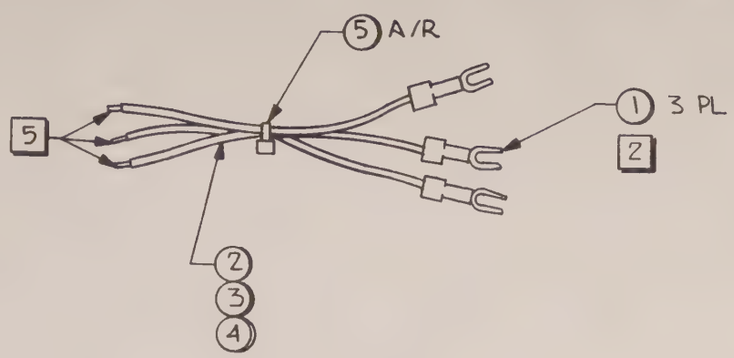
B 0117-0221 REV A

MODEL K105 SHEET 1 OF 1

KLINGLER K-VEL H 10

DWG. NO. 0117-0222 | SH 1 | REV. A

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50		PILOT REL PER ERN 309	STM		2-1-83
A	3957	PROD. REL PER ECO*	STM	DGW	9-16-83



2

WIRE NO	FROM	TO	AWG	COLOR	LENGTH
1	P/S -15V	-15V	16	VIO	4.0"
2	P/S 15V RET	15V RET	16	BLK	4.0"
3	P/S +15V	+15V	16	ORN	4.0"

5 STRIP INSULATION .25"

4. MANUFACTURE IN ACCORDANCE WITH WORKMANSHIP STD. 87000012.
3. BAG AND TAG WITH P/N 0117-0222, DASH NO AND REV LEVEL.
2 IDENTIFY PLUGS AND END OF WIRES WITH DESTINATION AS SHOWN
1. DRAWING IS TO SCALE AND MAY BE USED AS A TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES; XX ± .020 ± 1°; XXX ± .010
HOLE SIZE: 0 .599 ± .003; 600 .999 ± .004; 1.000-1.499 ± .005

	DRAWN	DATE
	STM	2-1-83
	CHECKED	
	PROD. ENG.	2/3/83
	MANUFACTURING	2-3-83
	QUALITY ASSUR	2-3-83

GOULD biomation

TITLE: MOTHER BOARD CABLE 15V

SCALE	SIZE	PART NUMBER	REV
1:1	B	0117-0222	A

CODE K105 | SHEET 1 OF 1

DASH NO.	NUMBER	QTY
10	0117-0045	1
	NEXT ASSEMBLY	

ENG. SERV. R. Kippen DATE 2/3/83

KLINGLER K-VEL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION
1									3	6200-0054-10	FORK LUG 14-16 AWG	
2									.5'	7150-0016-03	WIRE 16 AWG ORN	
3									.5'	7150-0016-07	WIRE 16 AWG VIO	
4									.5'	7150-0016-10	WIRE 16 AWG BLK	
5									AIR	7200-0008-10	CABLE TIE	

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD. REL PER ECO 3957	9-16-83	STM	DGW
50	PILOT REL PER ERN 309	2-1-83	STM	

DASH NO.	NUMBER	QTY
10	0117-0045	1
	NEXT ASSEMBLY	

		DATE
DWN	STM	2-1-83
CHK		
ENGR		2/3/83
MFG		2-3-83
Q.A		2-3-83

LIST OF MATERIAL
MOTHER BOARD CABLE 15V

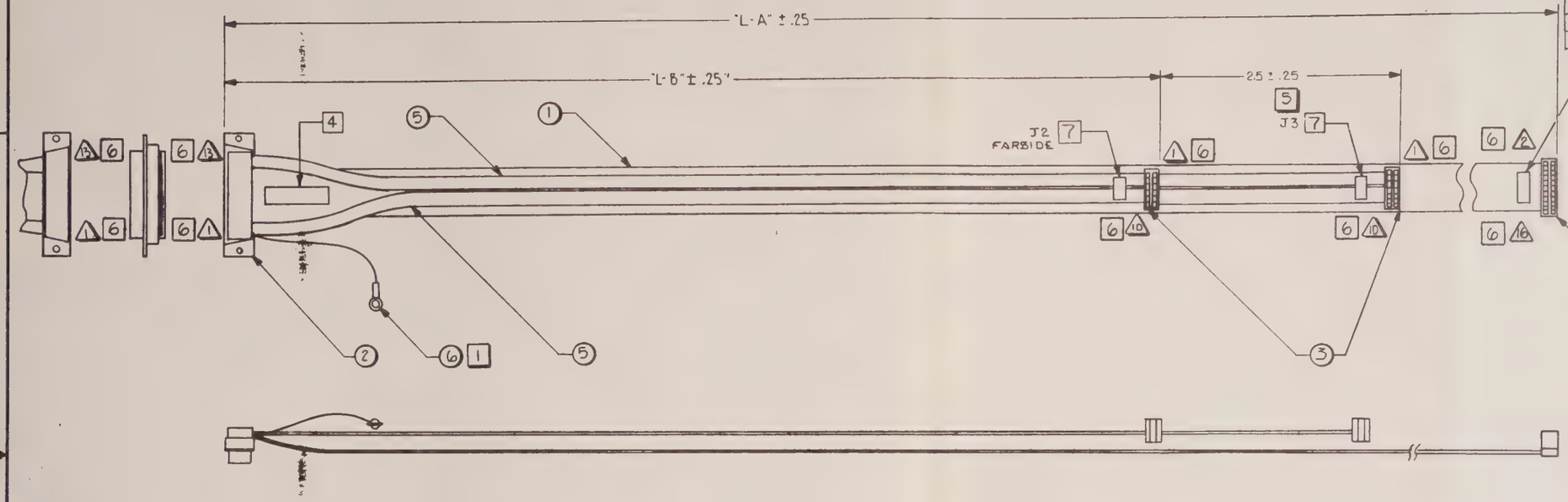
GOULD biomation

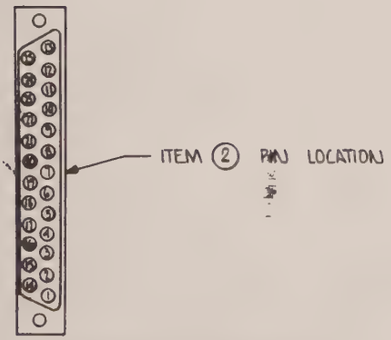
B | 0117-0222 | REV A

MODEL K105 | SHEET 1 OF 1

KLINGLER K-VEL H 10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	01		PROTOTYPE	STM		2-1-83
	02		REVISED	STM		2-2-83
	03		REVISED PIN OUTS ADDED DETAILS	STM		2-11-83
	04		REVISED ENG. ERROR	STM		2-14-83
	05		WIRE LIST HAD 2 PIN 183 REVISED LENGTH CLARIFIED NOTE 3, REVERSED ITEM 4	STM		3-1-83
	50		PILOT REL PER ERN 333	STM	[illegible]	3-30-83
	A	3957	PROD REL PER ECO#	STM	[illegible]	9-6-83
	B	4003	REVISED PER ECO Nº	JWC	[illegible]	10-18-83
	C	4580	PER ECO	[illegible]	[illegible]	[illegible]

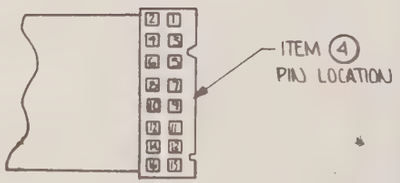


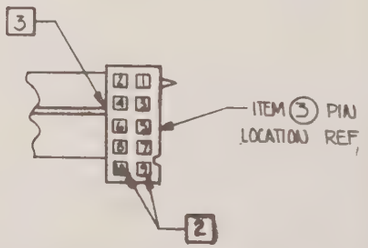


DASH Nº	L — A LENGTH	L — A DEST	L — B LENGTH	L — B DEST
01	80	HS CLK	40	J2, J3
02	80	HS F-8	40	J2, J3

WIRE LIST

CONN ITEM NO	PIN NO	COLOR	PIN NO	CONN. ITEM NO.
2	1	GREEN	—	6
	14	BIEGE	8	3
	2	YEL	7	3
	15	BIEGE	6	3
	3	ORN	5	3
	16	BIEGE	16	4
	4	GRAY	15	4
	17	BIEGE	14	4
	5	PURPLE	13	4
	18	BIEGE	12	4
	6	BLUE	11	4
	19	BIEGE	10	4
	7	GRN	9	4
	20	BIEGE	8	4
	8	YEL	7	4
	21	BIEGE	6	4
	9	ORN	5	4
	22	BIEGE	4	4
	10	RED	3	4
	23	BIEGE	2	4
	11	BRN	1	4
	24	BIEGE	4	3
	12	RED	3	3
	25	BIEGE	2	3
2	13	BRN	1	3
		N/C		3
		N/C		3





7 LABEL DESTINATION OF CABLES PER P/N CHART

6 △ DENOTES PIN NO. ON CONNECTOR

5 PLACE CONN'S ITEM ③ ON FLAT PORTION OF CABLE.

4. IDENTIFY WITH ASSY NO. 0117-0223, DASH NO. AND REV LEVEL

3 PIN / WIRE LOCATION IS IDENTICAL ON BOTH CONNECTORS ITEM ③ EXCEPT CONDUCTOR LOCATED BETWEEN PIN 6 ON BOTH CONNECTORS IS CUT.

2 PINS 9 AND 10 ARE NO CONNECTION

1 REMOVE 1ST CONDUCTOR (BIEGE) THEN PEEL AND CUT 2ND CONDUCTOR (GRN) TO LENGTH OF 4" AND INSTALL ITEM ⑥

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO	NUMBER	QTY
02	0117-0005	1
-01	0117-0005	1

NEXT ASSEMBLY

-06	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL X ± .1 ANGLES XX ± .020 ± 1° XXX ± .010 HOLE SIZE 0-500 ± .003 .005-.500 ± .004 1.000-1.400 ± .005

ENG SERV R. [illegible] DATE 4/10/83

DRAWN STM DATE 2-1-83

CHECKED [illegible] 4/13/83

[illegible] 4/13/83

MANUFACTURING [illegible] 4-13-83

QUALITY ASSUR [illegible] 4-14-83

GOULD Instruments Division Santa Clara Operations

TITLE CABLE KIT, HI-SPEED

SCALE NONE | SIZE D | PART NUMBER 0117-0223 | REV C

MODEL K105 | SHEET 1 OF 1

ITEM	QUANTITY PER ASSEMBLY								
	-90	-80	-70	-60	-50	-40	-30	-02	-01
1								7	7'
2								1	1
3								2	2
4								1	1
5								3.5	3.5
6								1	1
7									
8									
9									
10									

PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
7100-0068 -08	RIBBON CABLE, 8 PAIRS		
6000-0559-10	CONN. 25 PIN		
6000-0551-20	CONN. 10 PIN SOCKET		
6000-0352-20	CONN. 16 CONTACT SOCKET		
7100-0068-05	RIBBON CABLE, 5 PAIRS		
6200-0024-10	TERMINAL, RING TONGUE RED		

REV	DESCRIPTION	DATE	DWN	CKD
C	REVISED ECO 1580	7/5/84	GG	
	SEE HISTORY			

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
02	0117-0005	1
01	0117-0005	1

		DATE
DWN	STM	2.1.83
CHK		4/19/83
ENGR		4/13/83
MFG		4-13-83
Q.A		4/14/83

LIST OF MATERIAL

CABLE KIT,
HI-SPEED

GOULD biomation

B | 0117-0223 | REV C

MODEL K105 | SHEET 1 OF 1

LINGLER K-VEL H10

Gould, Inc.

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Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual: _____ How can this manual be improved: _____

_____

_____

Additional comments: _____

_____

Name _____ Department _____ M/S _____

Company: _____ Manual or Part No. _____

Address _____

City _____ State _____ Zip _____ Phone _____

Warranty/Registration

Please return this card to Gould, Inc. within five days

Did the packaging of this equipment exhibit any outward signs of physical damage ..... YES ○ ○ NO

Did this equipment arrive intact, without missing parts, loose parts or cable damage? ..... YES ○ ○ NO

Did the equipment operate on power-up? ..... YES ○ ○ NO

Did you attain adequate system performance? ..... YES ○ ○ NO

Were any electrical adjustments required? ..... YES ○ ○ NO

If you required assistance, was a local Gould, Inc. representative contacted? ..... YES ○ ○ NO

Comments _____

User Name _____ Title _____ Department _____ M/S _____

Company _____ Phone _____

Address _____ City _____ State _____ Zip _____

Model or Description _____ Serial or Part No. _____ Data Received _____

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